DELTA-SIGMA MODULATOR TOPOLOGIES FOR HIGH-SPEED HIGH-RESOLUTION A/D CONVERTERS

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ABSTRACT

By fully exploiting the enhanced stability characteristics of multibit quantization, stable higher-order ΔΣ modulators with finite-impulse-response (FIR) noise-transfer-functions (NTF) can be designed to achieve high signal-to-quantization-noise ratios at low oversampling ratios (OSR). This paper proposes a multibit ΔΣ modulator topology to realize FIR NTFs of arbitrary orders. Its key features include: reduced sensitivity to integrator nonlinearities, improved robustness to ΔΣ modulator coefficient variations, and decreased circuit complexity. Its performance is validated through simulations and compared to traditional ΔΣ modulator structures. This paper further discusses how the design of the signal transfer function (the signal path within the ΔΣ modulator) can significantly reduce the harmonic distortion due to opamp nonidealities in the modulator's loop filter and can help reduce the power dissipation, especially for high-speed high-resolution analog-to-digital converters (ADC) designed in low-voltage fine-line technologies.

I. INTRODUCTION

In today's telecommunications industry, the on-going research towards the development of A/D converters (ADCs) with higher speeds (> 2 MS/s) and higher resolutions (> 12 bits) is being equally driven by the demand for broadband wireline communication services (such as VDSL) as by the need for 3G wireless systems (such as UMTS). Oversampled ΔΣ ADCs can achieve a high-resolution A/D conversion of low-to-medium frequency signals. However, extending these converters to broadband applications requires lowering the oversampling ratio (OSR) in order to be realizable in the available IC technology and to meet the power budget. In a single-loop ΔΣ modulator (Fig. 1), the loss in signal-to-quantization-noise ratio (SQNR) due to the lowering of the OSR can be compensated for by increasing the noise-shaping order L of the loop filter H(z) and/or the resolution of the internal N-bit quantizer [1]. By fully exploiting the enhanced stability characteristics of multibit quantization (quantizer overload can be completely avoided, as discussed in Section V), stable higher-order ΔΣ modulators with aggressive noise-transfer-functions (NTFs) can be designed to achieve high SQNRs at low OSRs. This paper proposes a multibit ΔΣ modulator topology to realize finite-impulse-response (FIR) NTFs of arbitrary orders. Its key features include: reduced sensitivity to integrator nonlinearities, improved robustness to ΔΣ modulator coefficient variations, and decreased circuit complexity. While realizing high-performance NTFs has traditionally been the focus of ΔΣ modulator design, this paper further discusses how the design of the signal transfer function (STF) (i.e. the signal path within the ΔΣ modulator) can significantly reduce the harmonic distortion due to opamp nonidealities in the modulator's loop-filter [5] and can help reduce the power dissipation, especially for high-speed high-resolution ADCs designed in low-voltage fine-line technologies.

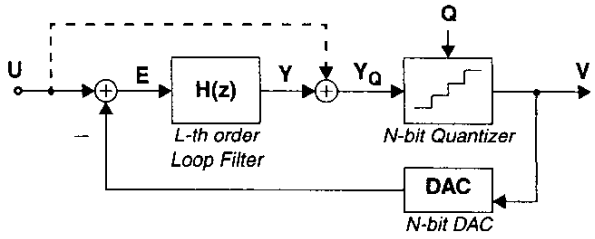

Fig. 1 Single-loop ΔΣ modulator. The feedforward path (dashed line) is used to achieve a unity-gain STF without affecting the NTF.

The paper structure is as follows: Next section briefly reviews FIR NTFs, while Section III describes the design of STFs. In Section IV, a multibit ΔΣ modulator topology is proposed and compared to traditional structures. Stability of higher-order ΔΣ modulators is discussed in Section V, before presenting simulation results to validate the performance of the proposed topology.

II. NOISE TRANSFER FUNCTION (NTF)

Consider the single-loop ΔΣ modulator modeled in Fig. 1, where the quantization noise is defined as $Q \equiv V - Y_Q$. The simplest NTF (from Q to V), which can achieve a high SQNR for high-order modulators even at a low OSR, is a high-pass FIR function with L zeros at dc ($z = 1$). For a given modulator order L, the attainable SQNR can be further increased by shifting a pair of complex-conjugate zeros to a frequency f_0, within the signal band $[0,f_B]$, in a manner that minimizes the inband quantization-noise power. For $L \geq 2$ and a sampling frequency of $f_s = 2\,f_B$ OSR, this corresponds to an NTF of the form

$$\mathrm{NTF} = (1 - z^{-1})^{L-2}(1 - \delta z^{-1} + z^{-2}) \qquad (1)$$

where $\delta \equiv 2\cos(2\pi f_0/f_s)$, and results in the high-pass NTF characteristic having a notch at frequency f_0. Assuming additive white quantization noise and a brick-wall decimation filter at the modulator's output, the optimal placement of the NTF complex-conjugate zeros is at approximately $f_0 = \sqrt{(2L-3)/(2L-1)}\ f_B$ and results in an SQNR improvement of over $20\log(L-0.5)$ dB. (For example, with $L = 4$, $f_0 = 0.845\,f_B$ results in an 11-dB SQNR improvement). Therefore, the excess SQNR gained by moving only one pair of complex-conjugate zeros closer to f_B, rather than spreading all the NTF zeros across the signal band [2], remains substantial and also independent of the OSR. Hence, this technique is particularly attractive for broadband applications where the OSR is inherently low. In practice, the position f_0 of the notch in the high-pass NTF should be optimized taking into account the non-ideal frequency response of the decimation filter. In general, simulations show that the SQNR sensitivity to the optimal f_0 is inherently low [3].

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III. .SIGNAL TRANSFER FUNCTION (STF)

The STF of the ΔΣ modulator modeled in Fig. 1 is

$$STF \equiv \frac{V}{U} = \frac{H}{1+H} = 1 - NTF, \qquad (2)$$

and the error signal at the input of the loop filter H(z) is

$$E \equiv U - V = (1 - STF)\,U - NTF\,Q. \qquad (3)$$

Accordingly, the FIR NTF in equation (1) results in an STF with a unity gain at low frequencies but with a high-pass characteristic. Depending on the OSR and L, this STF can be reasonably flat within the signal band. $[0,f_B]$: for $OSR \geq 8$ and $L \geq 3$, $-0.3dB \leq |STF| \leq 0.3dB$. Still, a flat (unity-gain) STF is more desirable because: a) it relaxes the requirements on the anti-alias filter preceding the modulator; and b) it enhances the modulator stability by reducing the out-of-band spectral components in the quantizer's input signal (due to electronic noise and when the modulator is driven by large transient signals with significant out-of-band energy), which may otherwise overload the quantizer.

In the ΔΣ modulator modeled in Fig. 1, a unity-gain STF,

$$STF = 1, \qquad (4)$$

can be achieved without affecting the NTF by adding the modulator's input signal to the quantizer's input signal [4,5], as shown by the feedforward path (the dashed line) in Fig. 1. As a result, the error signal entering the loop filter H(z) simplifies to

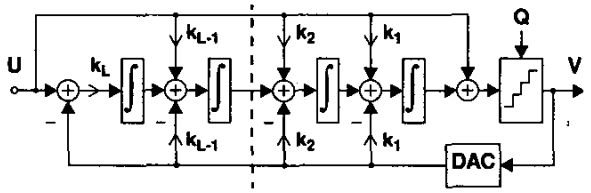
$$E = -NTF\,Q \qquad (5)$$

and, consequently, H(z) will only have to process shaped quantization noise. Since, ideally, no input signal is processed by the integrators of H(z), no harmonic distortion is generated. Accordingly, the modulator sensitivity to integrator nonlinearities, due to the nonlinear DC gain and the dynamic effects (finite bandwidth and slew rate) of the opamps in the integrators of H(z), is reduced [5,6]. The reduced distortion is particularly notable at low OSRs because: a) the sample-to-sample variations in the modulator's input signal U and, hence, in the error signal E are substantial (even more so with FIR NTFs whose large out-of band gains cause the un-filtered output waveform V to deviate from the desired waveform after the decimation filter by many LSBs); and b) the attenuation of the integrator nonidealities by the ΔΣ loop is inadequate in reducing the distortion appearing at modulator's output. For example, in the proposed ΔΣ modulator shown in Fig. 4 and discussed in Section IV, distortion at the output of integrator H_L will appear high-pass shaped by $1 - z^{-1}$ at the modulator's output and, therefore, attenuated by a factor of $2\sin(\pi/(2OSR))$ at $f = f_B$. Thus, for every factor of 2 lowering in the OSR, the attenuation of such distortion by the ΔΣ loop drops by about 6 dB.

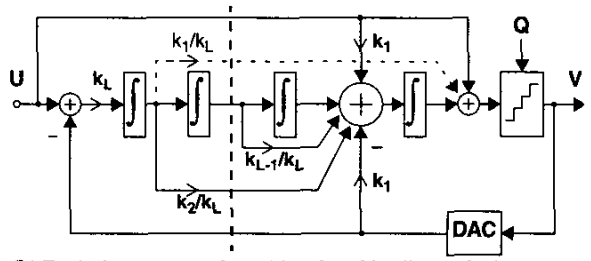
Further, by requiring the opamps in the integrators of the loop filter H(z) to process only shaped quantization noise, a significant reduction in the modulator's power dissipation can be achieved as:

a) the linearity requirements on the opamps are relaxed. Hence, by tolerating some gain and phase errors (due to finite opamp gains) in the transfer function of the integrators, opamps with only moderate gains can be used to realize the integrators. While moderate opamp gains (300 V/V) are readily obtainable in low-voltage fine-line technologies using classical folded-cascode or current-mirror opamp designs, high opamp gains require either additional gain stages or output-impedance enhancement. Both alternatives significantly increase the power dissipation and degrade the speed.

b) the available signal swing at the opamp outputs is no longer



(a) Adding feedforward paths to achieve an STF = 1.



(b) Equivalent structure but with reduced loading at the input.

Fig. 2 ΔΣ modulator with distributed feedback.

shared between the modulator's input signal U and the shaped quantization noise. Consequently, the maximum input-signal amplitude, $\|u\|_\infty \equiv \max|u|$, can be increased with respect to the output saturation voltage of the opamps, V_{sat}. In fact, the ΔΣ modulator can now tolerate an $\|u\|_\infty = V_{sat}$. (In ΔΣ modulators where the signal path goes through H(z), $\|u\|_\infty$ is typically set between 0.5 V_{sat} and 0.8 V_{sat} to avoid saturating the opamps). Let C_s denote the sampling capacitor used in the realization of the switched-capacitor (SC) integrator at the modulator's input. The sampling thermal (kT/C) noise of this integrator is typically the dominant noise source within the modulator [7]. Maximizing $\|u\|_\infty$ allows minimizing the C_s needed to lower the kT/C noise below the desired noise-floor for the modulator. Consequently, the power dissipation needed to achieve a given dynamic range is minimized [7]. Such power savings are particularly significant in low-voltage ADCs operating at low OSR because the inband power of the kT/C noise is inversely proportional to $\|u\|_\infty^2$ and the OSR.

In ΔΣ modulator topologies with distributed feedback [1,3], a unity-gain STF can be achieved without affecting the NTF by adding the modulator's input signal U to the outputs of the loop-filter integrators (as shown by the weighted feedforward paths in Fig. 2a) to cancel the spectral components of U at these nodes. Consequently, the loop-filter integrators will only have to process shaped quantization noise. However, to reduce the loading at the modulator's input, the distributed feedback paths can be replaced (without affecting the NTF) with feedforward paths [8,9] so that the input signal U needs to be added to only the outputs of the last two integrators, as shown in Fig. 2b without the feedforward path k_1/k_L.

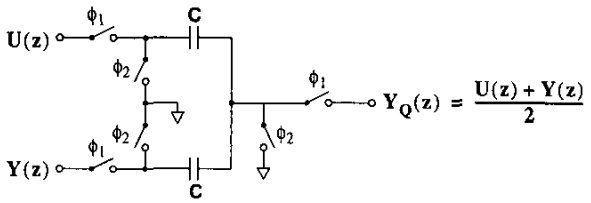
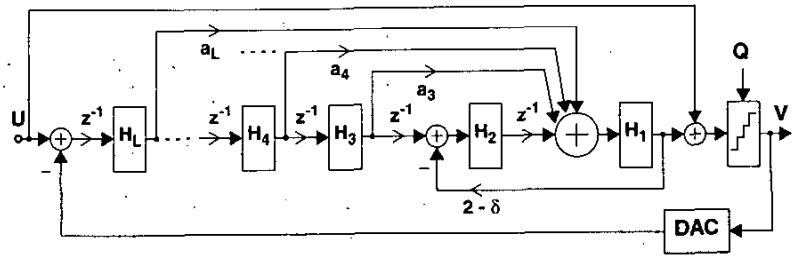
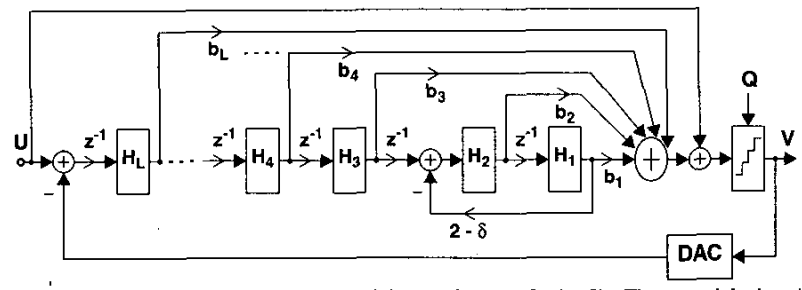


Fig. 3 SC realization of the summer at the quantizer input in Fig. 1.



L	a_3	a_4	a_5	a_6
3	δ + 1			
4	2 and $2z^{-1}$	δ + 2		
5	5	5	δ + 3	
6	4 and $2z^{-1}$	9	11	δ + 4

Fig. 4 Proposed ΔΣ modulator of order L (≥ 3). The non-delaying integrators are denoted by $H_i = 1/(1-z^{-1})$, i = 1, ..., L. The feedforward coefficients a_k, k = 3, ..., L, needed to realize the FIR NTF in equation (1) are given in the table. Note: for L = 4 (L = 6), path a_3 consists of two parallel paths: a non-delaying path with coefficient 2 (4) and a delaying path with coefficient $2z^{-1}$ ($2z^{-1}$).



L	b_1	b_2	b_3	b_4	b_5
2	δ−1	δ			
3	$\delta^2-\delta-1$	δ^2-1	δ + 1		
4	$\delta^3-\delta^2-2\delta+1$	$\delta^3-2\delta$	$\delta^2+\delta$	δ + 2	
5	$\delta^4-\delta^3-3\delta^2+2\delta+1$	$\delta^4-3\delta^2+1$	$\delta^3+\delta^2-\delta$	$\delta^2+2\delta+2$	δ+3

Fig. 5 Traditional feedforward ΔΣ modulator of order L (≥ 2). The non-delaying integrators are denoted by $H_i = 1/(1-z^{-1})$, i = 1, ..., L. The feedforward coefficients b_k, k = 1, ..., L, needed to realize the FIR NTF in equation (1) are given in the table.

This path (the dashed line) can be used to replace both the feedforward path k_1 and the feedback path k_1 in Fig. 2b. However, in this case, a weighted summation amplifier would be required at the quantizer's input.

In a SC implementation of the ΔΣ modulator in Fig. 1, the summation at the quantizer's input can be realized using a passive SC network [5], as shown in Fig. 3 (where a 2-phase non-overlapping clock is assumed). In this case, the quantizer overload ratio, A_{OL}, drops from $\|u\|_\infty/V_{ref}$ to $\|u\|_\infty/(2V_{ref})$, where V_{ref} is the quantizer reference signal. Therefore, to maintain the desired A_{OL}, V_{ref} must be scaled down by a factor of 2. However, this also scales down (by the same factor) the maximum acceptable accuracy for the comparators in the quantizer, thereby requiring higher-resolution comparators.

IV. PROPOSED ΔΣ MODULATOR TOPOLOGY

Fig. 4 shows a mathematical model of the proposed higher-order (L ≥ 3) single-loop ΔΣ modulator topology, which can be directly mapped to a SC circuit. Except for the finite-zero loop-gain parameter δ, the integrator coefficients needed to realize the FIR NTF in equation (1) are independent of the OSR and f_s. The implementation of the NTF complex-conjugate zeros is achieved by one additional local feedback around integrators H_1 and H_2 (thereby forming a resonator) and, hence, requires very little analog circuitry. To enhance the high-frequency settling properties, the proposed topology is designed with no delay-free loops and the integrators are interconnected such that the worst-case settling occurs when two opamps settle in series. Furthermore, in the proposed ΔΣ modulator topology, the D/A converter (DAC) needs only to feedback to the input stage. With multibit quantization, this significantly reduces the analog-circuit complexity, chip area, and power, especially if bootstrapped switches are needed in low-voltage designs.

The FIR NTF in equation (1) can also be implemented using the traditional feedforward ΔΣ modulator structure [1,10] as shown in Fig. 5. However, using the proposed topology (Fig. 4) offers the following advantages over the traditional feedforward structure (Fig. 5): i) the network complexity is reduced by not requiring a weighted summation amplifier before the quantizer; ii) the sensitivity of the ΔΣ modulator to variations in gains and integrator coefficients is significantly reduced, resulting in a more robust topology (as confirmed by the results in Section VI); and iii) after proper dynamic range scaling, the required modulator coefficients in the traditional feedforward structure (Fig. 5) have extremely small values compared to the proposed topology (Fig. 4), thereby introducing large capacitor-ratio spreads in SC implementations.

V. STABILITY

Assuming an STF = 1 and that the initial conditions of the ΔΣ modulator are such that the quantizer was not overloaded at anytime before time 0, a sufficient condition to guarantee that the N-bit quantizer will never overload [11] and, hence, ensure stability of the ΔΣ modulator, can be stated as

$$\frac{\|u\|_\infty}{V_{ref}} \le 1 - \frac{\|ntf\|_1 - 2}{2^N - 1} \tag{6}$$

where $\|ntf\|_1$ is the 1-norm (maximum instantaneous gain) of the NTF with impulse sequence ntf(n):

$$\|ntf\|_1 \equiv \sum_{n=0}^{\infty} |ntf(n)| = (2+\delta)\cdot 2^{L-2} \tag{7}$$

for the NTF in equation (1).

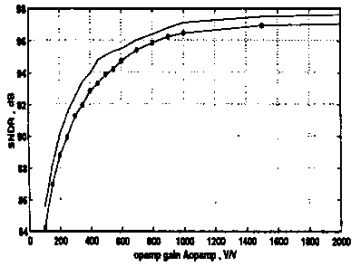


Fig. 6 SNDR versus A_{opamp} for the 3rd-order modulator with:
− $e_{max} = 0$ * $e_{max} = 2\%$

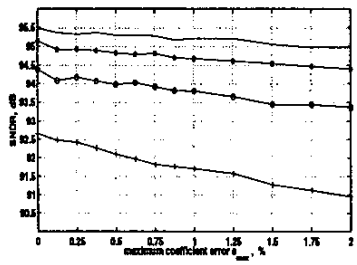


Fig. 7 SNDR versus e_{max} for the 4th-order modulator with:
− $A_{opamp} = \infty$ * $A_{opamp} = 60$ dB
o $A_{opamp} = 55$ dB + $A_{opamp} = 50$ dB

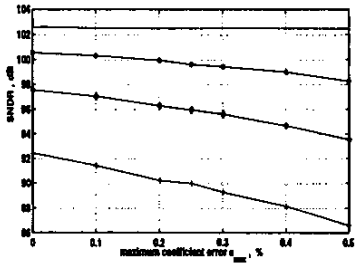


Fig. 8 SNDR versus e_{max} for the 5th-order modulator with:
− $A_{opamp} = \infty$ * $A_{opamp} = 60$ dB
o $A_{opamp} = 55$ dB + $A_{opamp} = 50$ dB

Furthermore, in order to preserve stability in actual circuit implementations, it is usually necessary to: i) scale the integrator coefficients in order to ensure that the peak integrator outputs are within the bounds dictated by the opamp saturation voltages; and ii) consider the combined effects of the nonlinear opamp gains and the ΔΣ modulator coefficient variations when determining $\|ntf\|_1$ and the corresponding maximum stable input range. These nonidealities can cause $\|ntf\|_1$ to increase and, hence, cause the modulator to become unstable, especially when designing for aggressive NTFs. In general, the stability test in equation (6) leads to a conservative upper bound on the maximum stable input [2]. Nonetheless, this test clearly reveals that, with proper design, stability is not a limitation to higher-order multibit ΔΣ modulators with FIR NTFs.

VI. SIMULATION RESULTS

The proposed ΔΣ modulator in Fig. 4 was simulated in MATLAB with the gain and phase errors (due to finite opamp gains) in the transfer function of the integrators modeled as described in [12]. The opamps were assumed to have a nonlinear gain corresponding to an input-output transfer curve in the form of a hyperbolic tangent with a maximum gain of A_{opamp} and an output saturation voltage of V_{sat}. The multibit DAC was assumed to be ideal. (However, in practice, dynamic element matching schemes and/or calibration techniques must be used to correct for the DAC nonlinearity due to static element mismatch errors [13]). A sine-wave signal with an amplitude of $\|u\|_\infty$ and a frequency of f_B was applied at the input. An f_s of 64 MHz was used. V_{ref} and V_{sat} were set to 1 V and 1.2 $\|u\|_\infty$, respectively. Dynamic range scaling was performed to ensure that the peak integrator outputs were at approximately $\|u\|_\infty/2$. The values of the signal-to-noise-plus-distortion ratio (SNDR) reported in this paper correspond to the minimum SNDR values found over 100 simulations in which each gain and integrator coefficient is assumed to have a uniformly-distributed random error in the range $\pm e_{max}$.

Fig. 6 shows the SNDR versus A_{opamp} of a 3rd-order modulator (with N = 5, OSR = 16, and $\|u\|_\infty$ = −2.5 dB) for various e_{max}. Accordingly, high resolution (SNDR > 14 bits) can be achieved with only moderate opamp gains (150 V/V). Fig. 7 and Fig. 8 show the SNDR versus e_{max} of, respectively, a 4th-order modulator (with N = 6, OSR = 8, and $\|u\|_\infty$ = −2.5 dB) and a 5th-order modulator (with N = 6, OSR = 8, and $\|u\|_\infty$ = −6 dB) for various A_{opamp}. Accordingly, these modulators could tolerate (in terms of stability) a maximum variation in gains and integrator coefficients of 2% and 0.5%, respectively. When the traditional feedforward structure in Fig. 5 was simulated under identical conditions (including comparable integrator output voltages), the range of e_{max} that guaranteed a stable modulator dropped to 0.75% and 0.2% for the 4-th and 5-th order modulators, respectively.

VII. CONCLUSION

A multibit ΔΣ modulator topology is proposed to realize FIR NTFs of arbitrary orders. Its key features include: reduced sensitivity to integrator nonlinearities, improved robustness to ΔΣ modulator coefficient variations, and decreased circuit complexity.

VIII. ACKNOWLEDGMENTS

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