A 1.8-V 3-MS/s 13-bit ΔΣ A/D Converter with Pseudo Data-Weighted-Averaging in 0.18-μm Digital CMOS

Anas A. Hamoui and Ken Martin

Dept. of Electrical and Computer Engineering, University of Toronto
10 King's College Road, Toronto, Ontario, M5S3G4 CANADA
{hamoui,martin}@eecg.toronto.edu

ABSTRACT

A 1.8-V ΔΣ modulator, fabricated in 0.18-μm standard digital CMOS process, achieves 81-dB SFDR and 74-dB SNR over a 3-MS/s conversion bandwidth. Its single-loop single-feedback architecture uses a 3rd-order FIR noise-transfer-function and a 5-bit quantizer to render the quantization noise negligible at 16x oversampling. A *pseudo* data-weighted-averaging technique linearizes the multibit feedback D/A converter, while eliminating the inband signal-dependent tones. The bootstrapped switches in the switched-capacitor implementation reduce the sampling distortion for a 1.85-V_{pp} input-signal range. The analog and digital power consumptions are 32.4mW and 12.6mW, respectively. The on-chip references dissipate 14.4mW.

I. INTRODUCTION

The development of A/D converters (ADCs) with higher speeds and higher resolutions is driven by the demand for high-speed instrumentation and broadband communication systems. Such ADCs must be implemented in standard digital CMOS processes for higher integration of the analog and digital functions and for reduced cost. However, the low supply-voltages in scaled CMOS processes limit the signal swing, thus complicating the design of low-power ADCs.

Extending oversampled ΔΣ ADCs to high-speed applications requires lowering ($\leq$ 16) the oversampling ratio (OSR) in order to be realizable within the technology limitations of submicron CMOS processes and to meet a moderate power budget. To maintain a high-resolution A/D conversion, the loss in signal-to-quantization-noise ratio (SQNR) due to OSR lowering can then be compensated for by increasing the order of noise-shaping and/or the number of quantization bits within the ΔΣ modulator. Other advantages of multibit quantization include enhanced modulator stability and relaxed slew-rate and settling requirements on the analog integrators. However, the linearity of a multibit ΔΣ modulator is limited by that of its multibit feedback D/A converter (DAC), thereby requiring linearization techniques to correct for the static mismatch errors in the DAC elements.

This paper describes a switched-capacitor (SC) ΔΣ modulator operating from a single 1.8-V supply and fabricated in a 0.18-μm standard digital CMOS process with no options for precision capacitors nor low-threshold voltages. It achieves a 13-bit spurious-free dynamic range (SFDR) and a 12-bit signal-to-noise ratio (SNR) over a 3-MS/s conversion bandwidth with a 1.85-V_{pp} input-signal range. Accordingly, for high-speed ($\geq$ 2MS/s) high-resolution ($\geq$ 12bits) applications, it is one of the few recently-reported [1,2] SC ΔΣ modulators operating from such a low supply-voltage. Through this experimental prototype, this work explores the design of SC ΔΣ modulators when the OSR and the supply voltage are limited by the technology. Namely:

i) Low-OSR High-SQNR ΔΣ Modulators: By fully exploiting the enhanced stability characteristics of multibit quantization, stable higher-order single-loop ΔΣ modulators with aggressive noise-transfer-functions (NTF) can be designed to achieve high SQNRs at low OSRs. Thus, the entire noise budget can be allocated to the analog noise sources (mainly, thermal kT/C noise) to reduce the power dissipation. Accordingly, a single-loop single-DAC-feedback ΔΣ modulator with a 3rd-order finite-impulse-response (FIR) NTF, a 5-bit quantizer, and a reduced circuit complexity compared to traditional feedforward modulators [3], is described in Section II. Its SC implementation, where bootstrapped switches are used to avoid the sampling distortion that limits the linearity and input-voltage range of low-voltage low-OSR ΔΣ modulators, is detailed in Section III.

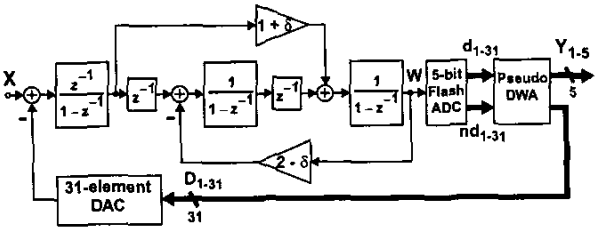

Fig. 1: ΔΣ modulator architecture.

ii) Pseudo DWA: A highly practical DAC linearization scheme, especially with a large number of DAC elements, is data weighted averaging (DWA) [4]. However, the occurrence of inband signal-dependent tones, when using DWA at low OSRs, degrades the SFDR and can preclude its use. This paper introduces a technique, called Pseudo DWA, to attenuate the DWA tones without sacrificing the SNR. Its implementation, described in Section IV, adds no extra delay in the ΔΣ feedback loop and requires only minimal additional digital-hardware and signal-processing compared to classical DWA.

The measured performance of the experimental ΔΣ modulator, including a comparison between the tone behavior of DWA and Pseudo DWA, is presented in Section V.

II. ΔΣ MODULATOR ARCHITECTURE

The single-loop single-DAC-feedback ΔΣ modulator in Fig. 1 is designed to realize a 3rd-order FIR NTF. Compared to traditional feedforward modulators [3], the circuit complexity is reduced by not requiring a weighted summation amplifier before the quantizer. With a single-loop topology, rather than a cascaded architecture, the ΔΣ modulator is much less sensitive to the finite dc gains of the opamps and, hence, is more suitable for low-power applications. Further, with a single DAC-feedback rather than a distributed DAC-feedback [5]: i) the output of only the last integrator becomes significantly correlated to the input signal, resulting in a lower distortion and a suppressed signal-swing at the output of the preceding integrators; and ii) the complexity of the analog circuit and DAC linearization is reduced, especially when using bootstrapped switches.

0-7803-7842-3/03/$17.00 © 2003 IEEE

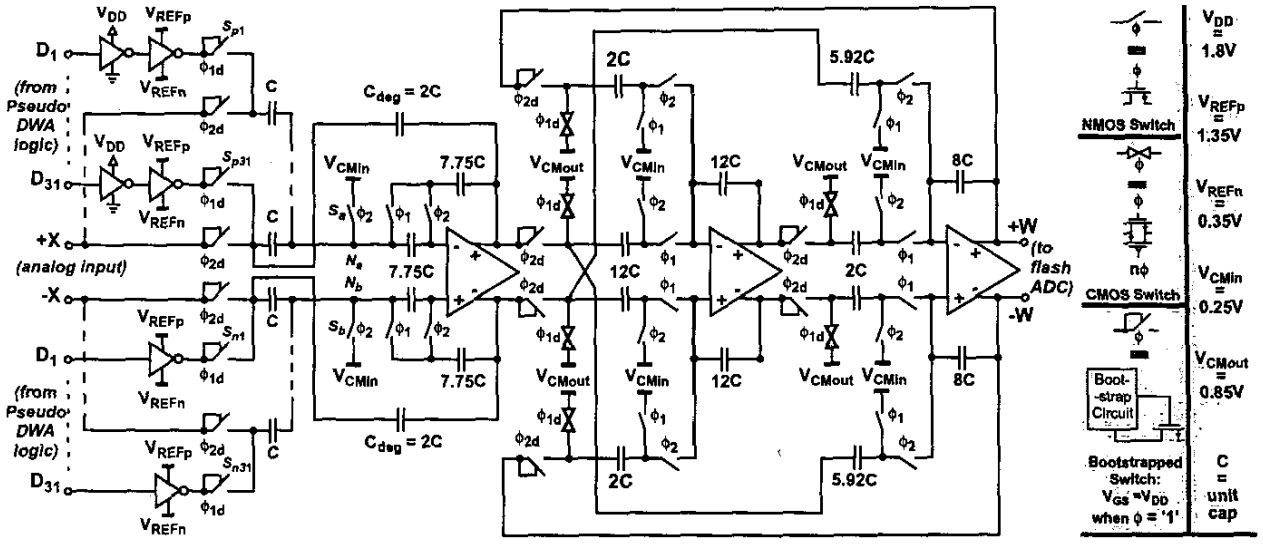

Fig. 2: Fully-differential SC implementation of the loop filter and the feedback DAC in the ΔΣ modulator of Fig. 1.

The FIR NTF is designed to have one zero at dc and two complex-conjugate zeros at $f_0 = (OSR/\pi)\ \text{acos}(\delta/2)\ f_B$, where f_B is signal-band edge. An $f_0 = f_B$ is chosen in order to achieve a more uniform quantization-noise across the signal band and to ease the requirements on the transition-band steepness of the output decimation-filter. A 5-bit quantizer, implemented as a 31-level flash ADC, is used to ensure that the 3rd-order modulator is stable for input signals close to full scale, while suppressing the quantization noise well below the thermal kT/C noise: the simulated ideal SQNR is 94dB for an OSR = 16 with $f_0 = f_B$ (i.e. $\delta = 1.96$).

III. Switched-Capacitor Implementation

Fig. 2 depicts the fully-differential SC implementation of the loop filter and the feedback DAC in the ΔΣ modulator of Fig. 1.

A. SC Integrators

The 1st integrator uses correlated double-sampling to minimize the errors due to the offset voltage, 1/f noise, and finite gain of the 1st opamp. Since similar errors in the succeeding amplifiers are suppressed by the gain of the preceding integrators, basic parasitic-insensitive structures are used for the 2nd and 3rd integrators. The integrator gains (Fig. 2) are optimally scaled to avoid clipping distortion in the opamps when operated from a 1.8-V supply and with an input-signal amplitude about 1.5dB below the output-saturation voltages of the opamps. Capacitor C_{deg} in the 1st integrator is a 'deglitching' capacitor used to provide continuous-time feedback during the non-overlap clock times when all switches are open.

B. Bootstrapped Switches

The switches in Fig. 2 are controlled by 2-phase non-overlapping clocks (ϕ_1,ϕ_2), and delayed clock phases (ϕ_{1d},ϕ_{2d}) are used to minimize the charge injection by the sampling switches. Nonetheless, bootstrapped switches were required to avoid any sampling distortion due to the signal-dependent on-resistance of the CMOS switches. Such distortion is particular significant in ΔΣ modulators designed: i) in scaled CMOS technologies, where the low supply-voltage is comparable to the sum of the NMOS and PMOS threshold voltages; and ii) at low-OSRs, where the sample-to-sample signal variations are substantial. Thus, to significantly improve the linearity of the sampling operation, NMOS bootstrapped switches [6] were used at the modulator's input, the integrators' outputs, and the DAC's outputs (Fig. 2). The latter were needed because the effective on-resistance of the DAC output switches ($S_{p1\text{-}31}$ and $S_{n1\text{-}31}$) is also signal-dependent: every clock cycle, each DAC switch can have one of two on-resistance values depending on whether it is passing V_{REFp} or V_{REFn}, and the number of DAC switches passing V_{REFp} (V_{REFn}) in the positive signal-branch does not necessarily equal that in the negative branch. Therefore, when the NMOS switches S_a and S_b in the 1st integrator are turned off at the end of ϕ_2, their surrounding impedance-environment and, hence, their charge injection into, respectively, nodes N_a and N_b are neither equal nor signal independent.

C. Opamps

Fig. 3 shows the schematic of the fully-differential opamp in the 1st integrator. It uses wide-swing cascode current-mirrors and a SC CMFB. Behavioral simulations indicate that a 50-dB dc gain is adequate as the ΔΣ architecture used is rather insensitive to finite opamp gains. The 1st opamp dissipates 7mA. Generally, in low-OSR ΔΣ modulators, scaling the bias current of the succeeding opamps is difficult because the attenuation of the integrator nonidealities by the ΔΣ loop is inadequate. However, since the 1st integrator has the largest gain (an advantage of feedforward topologies), the effective load-capacitances of the succeeding opamps are smaller, in spite of the last integrator driving the large input-capacitance of the flash ADC. This allowed scaling those opamps by 50% and saving power.

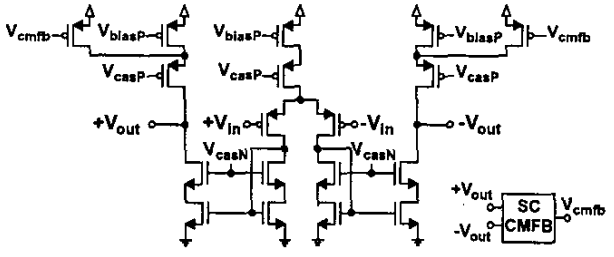

Fig. 3: Current-mirror opamp (biased using the circuit in Fig. 4).

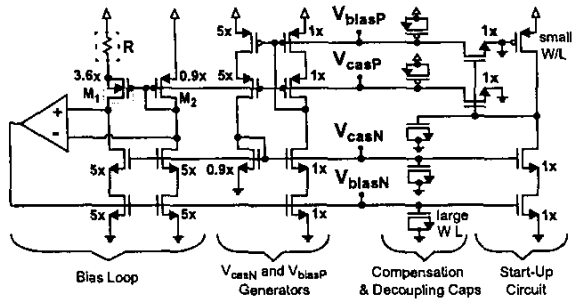

Fig. 4: Constant-gm bias circuit. The transistor multiplicative factors are relative to unit transistors with $W_{PMOS} = 4\ W_{NMOS}$.

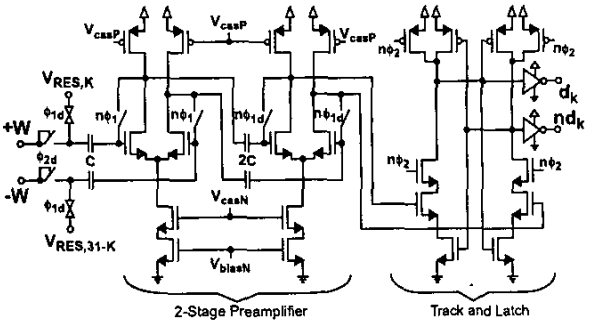

Fig. 5: K-th comparator in the flash ADC (K = 1, ..., 31). $V_{RES,n}$ is the reference voltage from the n-th node of the resistor string (n = 1, ...,31).

D. Bias Circuit

To minimize the dependency of the analog MOS circuits on process, supply voltage, and temperature, the constant-g_m bias circuit with an off-chip resistor R shown in Fig. 4 is used to provide the bias and cascode voltages for the current-mirror opamps (Fig.3) and to generate the reference voltages of the SC loop-filter (Fig.2). In Fig. 4, the differential amplifier forms a negative-feedback loop that controls V_{biasN} and keeps the drains of the Widlar current-mirror transistors (M_1-M_2) at equal potential. Furthermore, by connecting the well of M_1 to its source, its body effect is minimized and, hence, the M1-M_2 matching is improved. A transistor ratio M_1/M_2 of 4 sets the transconductance $g_{m2} \cong 1/R$. The other transistor ratios and the off-chip resistor R are sized to maximize the voltage swing at the opamps' outputs, while ensuring that all bias-circuit transistors are in saturation over all design corners and a worst-case 1.65-V supply.

E. Comparators

The 2-V_{pp} maximum output-swing of the opamps limits the input range of the 31-level flash ADC and, hence, bounds the nominal quantization step size to less than 32.25mV. Therefore, to minimize the quantization-level errors due to comparators' input offsets, a latched comparator with input offset-storage (shown in Fig.5) is used in the flash ADC. Delayed clock phases are used to minimize the charge injection by the sampling switches. Since the input capacitance C is not charged/discharged during operation (ignoring the leakage due to parasitic capacitances), the loading effect of the flash ADC on the SC loop-filter is small. The 2-stage preamplifier is biased using the circuit of Fig. 4 and its PMOS loads are accordingly sized for triode operation. It has an overall gain of 12V/V and dissipates 130μA. Furthermore, it helps prevent the track-and-latch kick-back-noise from entering the SC loop-filter and the resistor string which is used to generate the reference voltages $V_{RES,1\text{-}31}$ of the comparators. Inverters are inserted at the output of the track-and-latch stage [7] for buffering and to ensure a symmetrical load.

IV. Pseudo DWA

A dynamic element-matching technique, called Pseudo DWA, is introduced in this work to linearize the DAC. Pseudo DWA selects the DAC unit-elements in a rotational manner, as in conventional DWA [4], under the guide of an index pointer PTR. However, every n_{inv} clock-cycles, the least-significant bit (LSB) of the DAC input-code used to update PTR is inverted and, hence, a DAC unit-element is either skipped or re-selected depending on whether the previous DAC input-code was, respectively, even or odd. This simple modification to DWA breaks the cyclic nature of the DAC-element selection process and eliminates the inband signal-dependent DWA tones.

The choice of n_{inv} is a compromise between linearity and resolution: if n_{inv} is too large, the DWA tones will not be eliminated ($n_{inv} = \infty$ corresponds to conventional DWA); if n_{inv} is too small, different DAC elements will be used at significantly different rates, resulting in an increase in the inband DAC-mismatch noise. As confirmed by the experimental results in Section V, an $n_{inv} = 64$ is a good choice for improving the SFDR (more than 13-dB attenuation in DWA tones) without compromising the SNR (less than 1.5-dB drop).

The implementation of the Pseudo-DWA logic (shown in Fig. 6) is optimized for minimal delay in the ΔΣ feedback loop [5], as only clock-phase ϕ_1 is available for the flash-ADC output code to be generated, rotated, and D/A converted. A 5-stage logarithmic shifter rotates the 31-digit thermometer code $d_{1\text{-}31}$ from the flash ADC and generates an equivalent 31-digit code $D_{1\text{-}31}$, which is used to drive the DAC inverters in Fig. 2. Because the shifter outputs must be distributed over the entire chip to the local DAC inverters, buffers are inserted to deal with the gate and wiring capacitances: incomplete settling of any DAC inverter can lead to nonlinear distortion. The shifter is implemented using only NMOS transistors, with level restorers after the 3rd and 5th stages to achieve minimal delay. Its control signal (index pointer $PTR_{1\text{-}5}$) should be stable during phase ϕ_1 when the 31-digit code ripples through it. $PTR_{1\text{-}5}$ is updated every clock cycle as follows: **i)** the 31-digit thermometer code $d_{1\text{-}31}$ is converted to a 5-bit binary code $BIT_{1\text{-}5}$; **ii)** a 5-bit adder, with end-around carry, increments $PTR_{1\text{-}5}$ modulus 31 by $BIT_{1\text{-}5}$ and generates the index pointer to be used in the next ϕ_1 (next_$PTR_{1\text{-}5}$); **iii)** every 64 clock cycles, the LSB of $BIT_{1\text{-}5}$ is inverted before generating next_$PTR_{1\text{-}5}$. A 6-bit counter and a 2:1 mux control the timing of the LSB inversion. This is the only additional hardware required to implement Pseudo DWA instead of conventional DWA, and no extra delay is added in the critical feedback path (phase ϕ_1) of the ΔΣ loop.

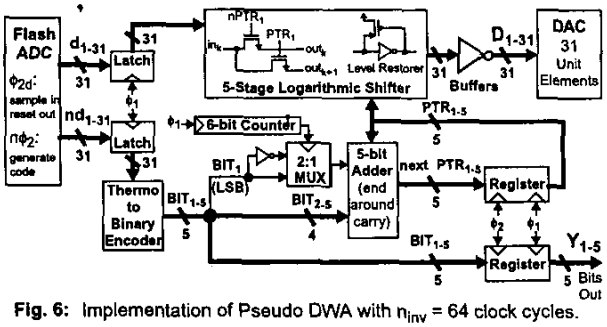

Fig. 6: Implementation of Pseudo DWA with $n_{inv} = 64$ clock cycles.

Table 1: Summary of measured ΔΣ-modulator performance.

Supply Voltage	1.8 V	**Signal Bandwidth**	1.5 MHz
Sampling Frequency	48 MHz	**Diff. Input Range**	1.85 V_{pp}
OSR	16	**Peak SFDR**	81 dB
Analog Power (1.8V)	32.4 mW	**THD**	-78 dB
Digital Power (1.8V)	12.6 mW	**DR**	75 dB
On-Chip References	14.4 mW	**Peak SNR**	74 dB
Area	4.2 mm^2	**Peak SNDR**	71 dB
Technology: 0.18μm 1-poly 6-metal standard digital CMOS			

V. Experimental Results

The ΔΣ modulator was fabricated in a 0.18-μm 1-poly 6-metal digital CMOS process with no options for precision capacitors nor low-threshold voltages. It occupies an active area of 4.2mm^2 (Fig. 9). The capacitors were realized using multiple unit-capacitors for accurate ratio-matching. Each unit capacitor was realized by stacking metals 2 to 5 in a woven structure for increased capacitance-density.

Post-fabrication simulations have demonstrated that the digital buffers in the Pseudo-DWA logic (Fig. 6) were under-designed because the wiring capacitances between the shifter outputs and the DAC inputs were under-estimated by the extractor. Consequently, the sampling frequency in this first experimental prototype had to be limited to 48MHz to achieve the desired linearity. However, the intended 64-MHz sampling-rate and the targeted 2-MHz signal-bandwidth should be achievable with only minor corrections. At a 48-MHz sampling rate, the measured performance of the ΔΣ modulator over a 1.5-MHz signal bandwidth is summarized in Table 1, and the SNR and SNDR are plotted in Fig. 7(a). When operated from a 1.8-V supply, the analog and digital power consumptions are 32.4mW and 12.6mW, respectively. The on-chip references dissipate 14.4mW.

In this experimental prototype, the Pseudo-DWA logic can be operated as classical DWA by disabling the counter in Fig. 6. Accordingly, the measured SFDR versus input levels is plotted in Fig. 7(b) for DWA and Pseudo DWA. Furthermore, to observe the DWA tones across the signal band, the output spectrum for a 25-kHz input is shown in Fig. 8 for: **(a) - 40-dBFS input:** here, the SFDR is limited by the large DWA tones near the signal-band edge, but it can be improved by 13dB using Pseudo DWA to attenuate these tones; **(b) - 1.67-dBFS input:** here, the SFDR is limited to 80dB by the nonlinear harmonic-distortion in the loop filter and is not improved by using Pseudo DWA, though the DWA tones are attenuated. The drops in the measured SNR and SNDR when using Pseudo DWA instead of DWA are only 1.5dB and 0.13dB, respectively.

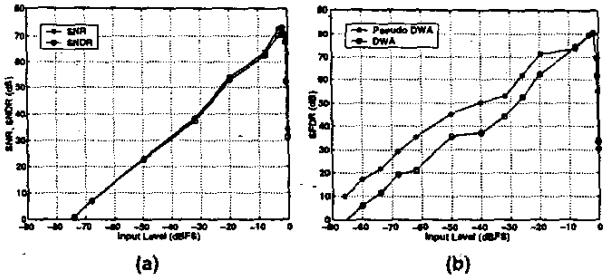

Fig. 7: (a) Measured SNR and SNDR vs. Input Level.
(b) Measured SFDR (Output Signal/Max. Spur) vs. Input

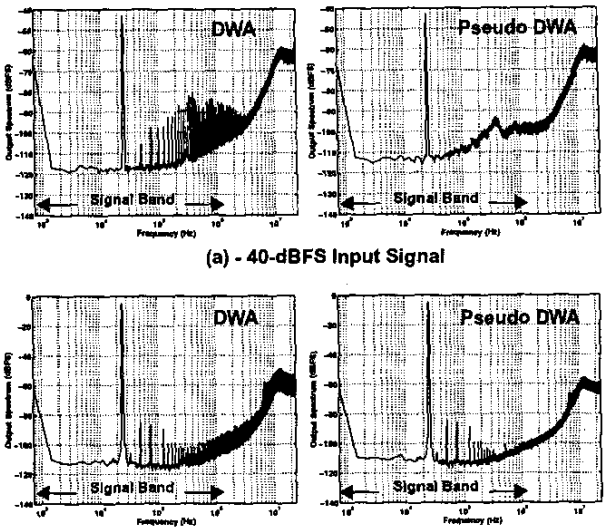

Fig. 8: Measured output spectrum when using DWA and Pseudo DWA.

VI. Conclusion

A 3rd-order single-loop multibit ΔΣ modulator was proposed for high-speed high-resolution applications where the supply voltage and the OSR are limited by the technology. Its SC implementation in a 1.8-V 0.18-μm standard digital CMOS process uses bootstrapped switches to achieve a 13-bit SFDR over a 3-MS/s conversion bandwidth and a 1.85-V_{pp} input-signal range. Furthermore, Pseudo DWA was experimentally demonstrated as a DAC-linearization technique suitable for low-OSR applications.

VII. References

[1] R. Jiang and T. S. Fiez, "A 1.8V 14b ΔΣ A/D converter with 4Msamples/s conversion," in *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 220-221.

[2] A. Dezzani and E. Andre, "A 1.2V dual-mode WCDMA/GPRS ΣΔ modulator," in *ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 58-59.

[3] P. Balmelli, Q. Huang, and F. Piazza, "A 50-mW 14-bit 2.5-MS/s Σ-Δ modulator in a 0.25mm digital CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2000, pp. 142-143.

[4] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, no. 12, pp. 753-762, Dec. 1995.

[5] Y. Geerts, M. J. Steyaert, and W. Sansen, "A high-performance multibit ΔΣ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829-1840, Dec. 2000.

[6] M. Dessouky and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched opamp circuits," *IEE Electronics Lett.*, vol. 35, no. 1, pp. 8-10, Jan. 1999.

[7] W-C Song, H-W Choi, S-U Kwak, and B-S Song, "A 10-b 20-Msample/s low-power CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 514-521, May 1995.

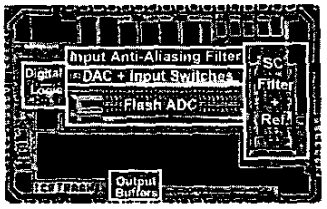

Fig. 9: Chip micrograph of the experimental ΔΣ modulator.