High-Order Multibit Modulators and Pseudo Data-Weighted-Averaging in Low-Oversampling $\Delta\Sigma$ ADCs for Broad-Band Applications

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***Abstract*—High-speed high-resolution $\Delta\Sigma$ analog-to-digital converters (ADCs) for broad-band communication applications must be designed at a low oversampling ratio (OSR). However, lowering the OSR limits the efficiency of a $\Delta\Sigma$ ADC in achieving a high-resolution A/D conversion. This paper presents several techniques that enable the OSR reduction in $\Delta\Sigma$ ADCs without compromising the resolution. 1) Noise transfer function (NTF). In this paper, a single-stage multibit $\Delta\Sigma$ modulator with a high-order finite-impulse-response NTF is proposed to achieve high signal-to-quantization-noise ratios at low OSRs. Its key features include: decreased circuit complexity, improved robustness to modulator coefficient variations, and reduced sensitivity to integrator nonlinearities. Its performance is validated through behavioral simulations and compared to traditional $\Delta\Sigma$ modulator structures. 2) Signal transfer function (STF). This paper describes how the STF of a $\Delta\Sigma$ modulator can be designed, independently of the NTF, in order to significantly reduce the harmonic distortion due to opamp nonidealities and to help lower the power dissipation. 3) Dynamic element matching (DEM) is also presented. Data weighted averaging (DWA) has prevailed as the most practical DEM technique to linearize the internal digital-to-analog converter (DAC) of a multibit $\Delta\Sigma$ modulator, especially when the number of DAC elements is large. However, the occurrence of in-band signal-dependent tones, when using DWA at a low OSR, degrades the spurious-free dynamic range. This paper proposes a simple technique, called Pseudo DWA, to solve the DWA tone problem without sacrificing the signal-to-noise ratio. Its implementation adds no extra delay in the $\Delta\Sigma$ feedback loop and requires only minimal additional digital hardware. Existing schemes for DWA tone reduction are also compared.**

***Index Terms*—$\Delta\Sigma$ modulators, analog-to-digital converters (ADCs), data-weighted averaging (DWA), digital-to-analog conversion, dynamic element matching (DEM), mismatch shaping.**

I. Introduction

THE evolving research toward the development of A/D converters (ADCs) with higher speeds and higher resolutions is being equally driven by the demand for high-speed wireline communication services (as in xDSL modems) as by the need for broadband wireless systems (as in 3G and 4G mobile terminals). Oversampled $\Delta\Sigma$ ADCs are well known for their ability to achieve a high-resolution A/D conversion in low-to-medium speed applications [1]. However, extending these converters to broadband applications requires lowering the oversampling ratio (OSR) in order for the $\Delta\Sigma$ modulator to be realizable within the technology limitations of submicron CMOS processes and to meet a moderate power budget.

Consider the single-stage $\Delta\Sigma$ modulator depicted in Fig. 1, with OSR $\equiv f_S/(2f_{\rm BW})$ where f_S is the sampling frequency and $[0, f_{\rm BW}]$ is the frequency band of the analog input signal. The loss in the signal-to-quantization-noise ratio (SQNR) due to the lowering of the OSR can be compensated for by increasing the noise-shaping order L of the loop filter $H(z)$ and/or the resolution of the B-bit quantizer. The impact of increasing the order L on the SQNR diminishes significantly as the OSR is reduced. In contrast, the effectiveness of increasing the number of quantization bits B is independent of the OSR. Other advantages of multibit quantization include enhanced modulator stability as well as relaxed slew-rate and settling requirements on the operational amplifiers (opamps) of the loop-filter integrators. However, the linearity of a multibit $\Delta\Sigma$ modulator is limited by that of its multibit feedback D/A converter (DAC), thereby requiring linearization techniques to correct for the mismatch errors in the DAC elements.

Table I summarizes the architecture and performance of published $\Delta\Sigma$ ADCs which are fabricated in a submicron CMOS technology and which are intended for high-speed (signal bandwidth $f_{\rm BW} \geq 1$MHz) and high- resolution (dynamic range DR and/or spurious-free dynamic range SFDR$\geq$ 12 bits) applications. Observe that all the high-speed high-resolution $\Delta\Sigma$ ADCs with multibit $\Delta\Sigma$ modulators reported in Table I rely (except [3]) on data weighted averaging (DWA) [25] or a modified version of DWA in order to linearize their internal multibit DACs. DWA is a highly practical and effective dynamic-element-matching (DEM) technique to implement, especially when the number of DAC elements is large. However, at a low OSR, the DWA algorithm must be modified to prevent the occurrence of in-band signal-dependent tones in the output spectrum of the $\Delta\Sigma$ modulator. Although the tone problem of DWA can be circumvented by the modified DWA techniques that have been recently proposed [8], [12], [14], [19], [23], [27], [28], these techniques can significantly degrade the achievable signal-to-noise-plus-distortion ratio (SNDR) or may still generate notable inband tones.

This paper presents several techniques that enable the reduction of the OSR in discrete-time $\Delta\Sigma$ modulators without compromising the resolution:

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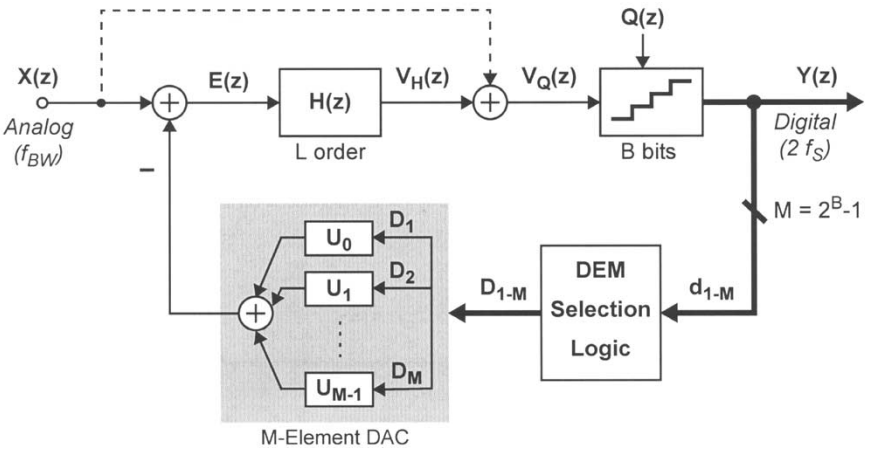

Fig. 1. Linear model of a single-stage $\Delta\Sigma$ modulator with a single DAC feedback. Dynamic element matching (DEM) is used to linearize the multibit feedback DAC. The feedforward path (dashed line) can be used to acheive an STF$=1$ without affecting the NTF.

1) **Noise Transfer Function (NTF):** By fully utilizing the enhanced stability characteristics of multibit quantization, stable high-order $\Delta\Sigma$ modulators with aggressive NTFs can be designed to achieve a high SQNR at a low OSR. Thus, the noise budget of a switched-capacitor (SC) $\Delta\Sigma$ modulator can be almost entirely allocated to the analog noise sources (mainly, the sampling kT/C noise) in order to minimize the power dissipation. Accordingly, this paper proposes a multibit $\Delta\Sigma$ modulator architecture to realize finite-impulse-response (FIR) NTFs of arbitrary orders. Its key features include: decreased circuit complexity, improved robustness to modulator coefficient variations, and reduced sensitivity to integrator nonlinearities.
2) **Signal Transfer Function (STF):** The focus of $\Delta\Sigma$ modulator design has traditionally been on realizing NTFs which can achieve a high SQNR without destabilizing the modulator. This paper describes how the design of the STF can be utilized, independently of the NTF, in order to significantly reduce the harmonic distortion due to opamp nonidealities in the loop-filter integrators [31] and to help lower the power dissipation.
3) **Dynamic Element Matching (DEM):** The occurrence of in-band signal-dependent tones, when using DWA at a low OSR, degrades the SFDR of the $\Delta\Sigma$ modulator and can preclude using DWA in low-oversampling $\Delta\Sigma$ ADCs. This paper proposes a simple technique, called Pseudo DWA, to remedy the tone behavior of DWA without sacrificing the SNDR. Its implementation adds no extra delay in the $\Delta\Sigma$ feedback loop and requires only minimal additional digital-hardware and signal-processing compared to conventional DWA.

The outline of this paper is as follows. Section II describes the design of the STF to minimize the sensitivity of $\Delta\Sigma$ modulators to integrator nonidealities. Section III briefly reviews FIR NTFs and examines the stability of multibit $\Delta\Sigma$ modulators. In Section IV, a single-stage multibit $\Delta\Sigma$ modulator architecture is proposed to realize FIR NTFs of arbitrary orders and its performance is compared to traditional structures. In Section V, the DWA algorithm is briefly reviewed before analyzing the DWA tone behavior. In Section VI, Pseudo DWA is proposed to eliminate the tones in conventional DWA, its performance is compared to previously reported schemes for DWA tone reduction, and its implementation in a test-chip $\Delta\Sigma$ ADC is described.

II. Design of the STF

A. Advantages of a Unity-Gain STF

The noise and signal transfer functions of the $\Delta\Sigma$ modulator modeled in Fig. 1 are, respectively, defined as

$$\text{NTF}(z) \equiv \frac{Y(z)}{Q(z)} = \frac{1}{1+H(z)} \tag{1}$$

$$\text{STF}(z) \equiv \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = 1 - \text{NTF}(z) \tag{2}$$

where $Q(z) \equiv Y(z) - V_Q(z)$ is the quantization noise. The error signal at the input of the loop filter $H(z)$ is

$$\begin{aligned} E(z) &\equiv X(z) - Y(z) \\ &\equiv [1 - \text{STF}(z)]X(z) - \text{NTF}(z)Q(z). \end{aligned} \tag{3}$$

Therefore, a unity-gain STF

$$\text{STF}(z) = 1 \tag{4}$$

reduces the error signal entering the loop filter to

$$E(z) = -\text{NTF}(z)Q(z). \tag{5}$$

Consequently, the loop filter $H(z)$ will only have to process shaped quantization noise. Since, ideally, no input signal is processed by the loop-filter integrators, no harmonic distortion is generated. Accordingly, the modulator sensitivity to integrator nonlinearities, due to the nonlinear dc gain and the dynamic effects (finite bandwidth and slew rate) of the opamps in the loop-filter integrators, is reduced [30], [31].

TABLE I
PUBLISHED $\Delta\Sigma$ ADCS WHICH ARE DESIGNED FOR HIGH-SPEED ($f_{\mathrm{BW}} \geq 1$ MHz) HIGH-RESOLUTION (DR AND/OR SFDR $\geq$ 12 bits) APPLICATIONS AND FABRICATED IN A SUBMICRON CMOS TECHNOLOGY

Ref.	$2f_{BW}$ (MS/s)	Supply[a] (V)	Power (mW)	*DR* (dB)	Peak *SFDR* (dB)	Peak *SNR* (dB)	Peak *SNDR* (dB)	CMOS Process[b]	Area (mm^2)	$\Delta\Sigma$ Modulator Architecture[c]	DEM	*OSR*
Marques 98 [4]	2	5	230	91				1μm 2P		2-1-1		24
Philips 03 [22]	2	1.8	4.4	76			76	0.18μm 1P5M	0.22	Complex ΔΣ 5(1b) Continuous-Time		32
Balmelli 00 [10][16]	2	2.5	50	86		80	78	0.25μm 1P6M	1.1	5(1.5b) SF		32
Brandt 91 [2]	2.1	5	41	74				1μm 1P		2-1(3b)		24
Wiesbauer 99 [7]	2.2	3.3	165	90		83		0.6μm	2.6	2(3b)-1(5b)		12
Medeiro 99 [5]	2.2	+2 -2	55	79				0.7μm 1P		2-1-1(3b)		16
Del Rio 01 [13]	2.2	3.3	78	81				0.35μm 1P	1.3	2-1-1(4b)		16
Geerts 99 [6]	2.2	3.3	200	92				0.5μm 2P		2-1-1		24
Morizio 00 [11]	2.2	A: 3.0 D: 2.5	187			81	72	0.35μm 2P3M	3.6	2-2(5b)		24
Morizio 00 [11]	2.2	A: 3.0 D: 2.5	248			86	79	0.35μm 2P3M	4.3	2-2-2		24
Gupta 02 [18]	2.2	3.3	180		106	88	88	0.18μm 1P5M Dual-Gate Oxide	2.6	2-1-1(2b)		29
Yan 03 [21]	2.2	3.3	62	88	93	84	83	0.5μm 2P3M	5.76	3(5b) Continuous-Time		16
Kuo 02 [14]	2.5	2.5	105	84	90		80	0.25μm 1P5M MIM Caps	2.6	4(4b) SF	Incremental DWA	12
Brooks 97 [3]	2.5	A: 5 D: 3	550	89		89		0.6μm 2P	35.3	2(5b) and 12-b Pipelined	Butterfly Shuffler	8
Fujimori 00 [8]	2.5	A: 5 D: 3	105		102	90		0.5μm 2P3M	24.8	2(4b)-1(4b)-1(4b)	Bi-directional DWA	8
Geerts 00 [9]	2.5	5	295	97	103	95	89	0.65μm 2P	5.3	3(4b) DF	DWA	24
Hamoui 03 [24]	3	1.8	45	75	81	74	71	0.18μm 1P6M	4.2	3(5b) SF	Pseudo DWA	16
Miller 02 [19]	3.84	2.7	50			70		0.18μm Dual-Gate Oxide	1.4	2(6b) DF	Rotated DWA	12
Veldhoven 03 [20][17]	3.84	1.8	4.5	74		74		0.18μm 1P5M	0.18	5(1b) Continuous-Time		40
Del Rio 01 [13]	4	3.3	78	75				0.35μm 1P	1.3	2-1-1(4b)		16
Kuo 02 [14]	4	2.5	105	80	85		74	0.25μm 1P5M MIM Caps	2.6	4(4b) SF	Incremental DWA	12
Jiang 02 [15]	4	1.8	150	83	103		82	0.18μm 2P5M	2.9	5(4b) SF	DWA	8
Vleugels 01 [12]	4	2.5	150	95	90	90	87	0.5μm 2P3M	10	2(5b)-2(3b)-1(3b)	Partitioned DWA	16
Park 03 [23]	5	A: 5 D: 3	495		106	89	88	0.35μm 2P4M	12.3	2(3b)-1(4b)-1(4b)	Randomized DWA	8
Geerts 00 [9]	12.5	5	380	71	82	68	67	0.65μm 2P	5.3	3(4b) DF		8

Supply Voltage: A = analog and D = digital power-supply voltages.
CMOS Process: $xPyM$ = CMOS process with x poly layers and y metal layers.
$\Delta\Sigma$ **Modulator Architecture**: Unless otherwise specified, the $\Delta\Sigma$ modulators have a discrete-time architecture. $L(Bb)$ = L-order B-bit single-stage modulator. $L_1(B_1b) - L_2(B_2b) - L_3(B_3b)$ = cascaded structure with L_1-order B_1-bit,L_2-order B_2-Bit, and L_3-order B_3-bit modulator stages. SF = single-DAC-feedback and DF = distributed-DAC-feedback architecture.

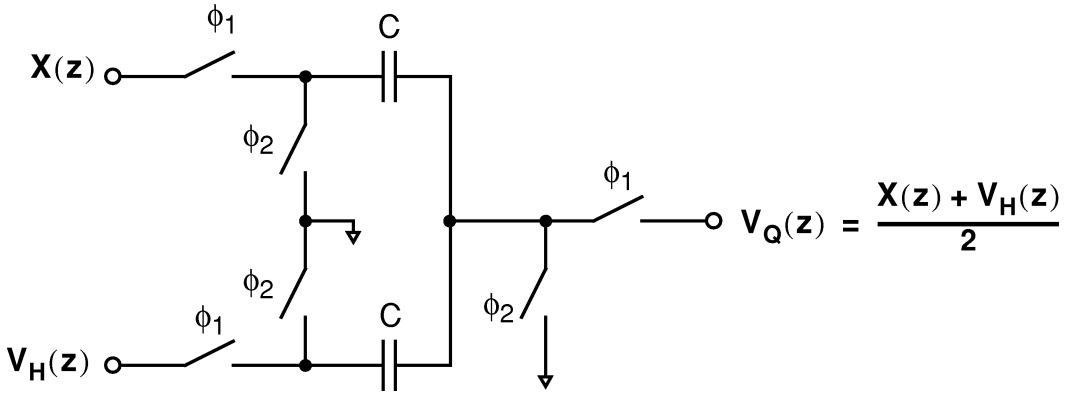

Fig. 2. SC realization of the summation at the quantizer input in Fig. 1.

The reduced distortion, achieved by designing the $\Delta\Sigma$ modulator for an STF$=1$, is particularly notable **at a low OSR** for the following reasons.

1) The sample-to-sample variations in the modulator's input signal X and, hence, in the error signal E are substantial at a low OSR. It is even more so with an FIR NTF (discussed in Section III) whose large out-of-band gain amplifies the out-of-band noise and causes the unfiltered output waveform Y to deviate by many least-significant bits (LSBs) from the desired output waveform after the decimation filter [33].
2) The attenuation of the integrator nonidealities by the $\Delta\Sigma$ loop is inadequate in reducing the distortion appearing at the modulator output Y at a low OSR. For example, consider the first integrator stage at the input of the loop filter. Assume that this integrator stage has a gain k_1. Furthermore, assume that the distortion error at its output can be modeled as a white noise. Such distortion error will appear high-pass filtered by $(1-z^{-1})/k_1$ at the output of the $\Delta\Sigma$ modulator and, therefore, attenuated by a factor of approximately $\pi^2/(3k_1^2\text{OSR}^3)$ within the signal band. Thus, for every factor of 2 lowering in OSR, the attenuation of such distortion error by the $\Delta\Sigma$ loop drops by about 9 dB.

Furthermore, by designing the $\Delta\Sigma$ modulator for an STF $=1$ and, hence, requiring the opamps in the integrators of the loop filter $H(z)$ to process only shaped quantization noise, a significant **reduction in power dissipation** can be achieved for the following reasons.

1) **Modulation Input-Signal Range:** The available signal swing at the outputs of the opamps is no longer shared between the modulator input signal and the shaped quantization noise. For example, with STF$(z)=1$ in Fig. 1, the loop-filter output reduces to $V_H(z)=-H(z)\text{NTF}(z)Q(z)$ and, hence, becomes independent of the modulator input signal $X(z)$. As a result, the maximum amplitude [1] $\|x\|_\infty$ of $X(z)$ is no longer limited by the available swing for $V_H(z)$. Hence, $\|x\|_\infty$ can be increased with respect to the output saturation voltage $V_{O,\text{sat}}$ of the opamp in the last integrator of the loop filter. In fact, the modulator can now tolerate an $\|x\|_\infty = V_{O,sat}$. In contrast, $\Delta\Sigma$ modulators whose signal path goes through $H(z)$ are typically designed for an $\|x\|_\infty$ between 0.5 and 0.8 $V_{O,\text{sat}}$ to avoid saturating the opamps [1]. Furthermore, an SC $\Delta\Sigma$ modulator is designed such that the kT/C noise of the sampling switches in the first integrator stage at the modulator input is the dominant noise source within the modulator[8]. Thus, maximizing $\|x\|_\infty$ allows minimizing the input sampling capacitor needed to lower the kT/C noise below the desired noise-floor for the modulator. Consequently, the power dissipation needed to achieve a given dynamic range is minimized [36]. Such power savings are particularly significant in low-voltage low-oversampling ADCs because the in-band signal-to-noise ratio due to the kT/C noise is inversely proportional to $\|x\|_\infty^2$ and OSR.
2) **Opamp DC Gain:** The linearity requirements on the opamps are relaxed. Hence, by tolerating some gain and phase errors (due to the finite opamp gains) in the transfer function of the integrators, opamps with only moderate gains can be utilized to realize the integrators. While opamps with moderate dc gains (150 to 300 V/V) are readily obtainable using classical folded-cascode or current-mirror designs, high-gain opamps require either multiple gain stages or output-impedance enhancement [35] because of the shrinking supply voltages and the poor intrinsic gains of the MOS transistors in scaled CMOS technologies. Such gain-boosting techniques for the opamps significantly increase the power dissipation and degrade the speed.
3) **Opamp Slew Rate:** The signal-path delay is reduced to zero. Decreasing the number of delays in the signal path decreases the sample-to-sample variations in the error signal E at the loop-filter input. As a result, for a targeted settling performance in the SC integrators of the loop filter (especially in the first integrator stage which has the largest impact on the overall modulator performance), the required slew rate and, hence, power dissipation in the opamps are relaxed [12]. In a single-stage $\Delta\Sigma$ modulator, the number of delays in the signal path is typically equal to the noise-shaping order L of the loop filter. However, by designing the $\Delta\Sigma$ modulator for an STF$=1$, the signal-path delay can be reduced to zero. Ac-

[1] $\|x\|_\infty = \max[|x(n)|]$

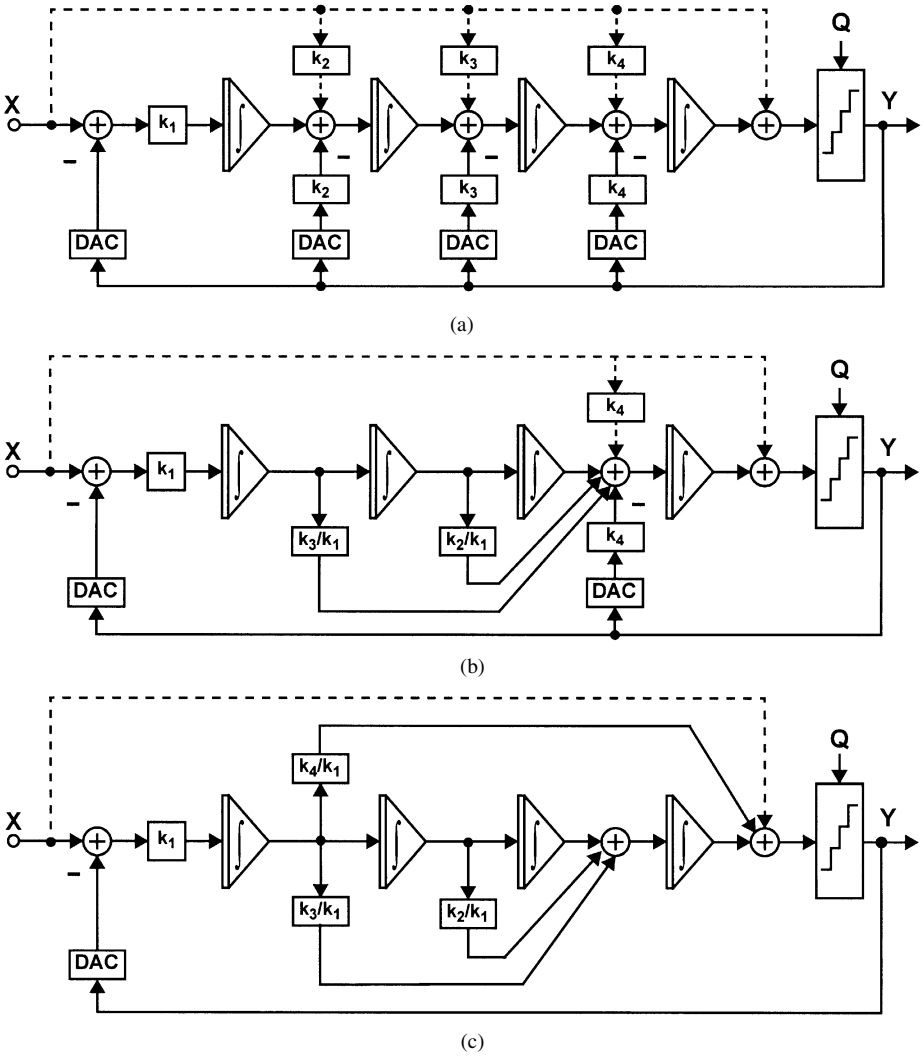

Fig. 3. (a) Fourth-order $\Delta\Sigma$ modulator with a distributed DAC feedback. The dashed feedforward paths are used to achieve an STF $= 1$, without affecting the NTF. (b), (c) The feedback paths of the modulator in (a) are replaced with feedforward paths, without affecting the NTF. The dashed feedforward paths are then used to achieve an STF $= 1$, resulting in modulator topologies that are equivalent to (a) but with reduced input loading.

cordingly, high-order single-stage $\Delta\Sigma$ modulators can be realized without increasing the requirements of the slew rate and, hence, power dissipation in the opamps of the SC integrators.

In summary, designing a $\Delta\Sigma$ modulator with an STF $= 1$ is generally more desirable than any other STF characteristic because it significantly reduces the sensitivity of the $\Delta\Sigma$ modulator to integrator nonidealities (as the analog input signal does not flow through the loop filter) and, hence, helps minimizing the power dissipation.

B. Unity-Gain STF in a Single-Feedback $\Delta\Sigma$ Modulator

In a $\Delta\Sigma$ modulator with a single DAC feedback (i.e., a single-loop $\Delta\Sigma$ modulator), an STF $= 1$ can be achieved without affecting the NTF by adding the modulator's input signal to the quantizer's input signal [31], [32], as shown by the feedforward path (the dashed line) in Fig. 1.

In an SC realization of the $\Delta\Sigma$ modulator in Fig. 1, the summation at the quantizer input can be implemented using an SC network [31], as shown in Fig. 2 where a two-phase nonoverlapping clock is assumed. However, such passive implementation entails a factor of two drop in the quantizer's input signal V_Q. Therefore, in order to maintain the desired performance for the $\Delta\Sigma$ modulator, the quantizer's reference voltage $V_{\rm ref}$ must be scaled down by a factor of two from its nominal value. However, this also scales down (by the same factor) the quantizer's step size and, hence, the maximum acceptable accuracy for the comparators in the quantizer. Accordingly, comparators with a higher resolution will be required.

C. Unity-Gain STF in a Distributed-Feedback $\Delta\Sigma$ Modulator

In a $\Delta\Sigma$ modulator with a distributed DAC feedback (i.e., a multiloop $\Delta\Sigma$ modulator) [9], [37], an STF $= 1$ can be achieved without affecting the NTF by adding the modulator's input signal X to the outputs of the loop-filter integrators, as shown by the weighted feedforward paths (dashed lines) in Fig. 3(a). This cancels the spectral components of X at these nodes and, consequently, the loop-filter integrators will only have to process shaped quantization-noise. However, this technique significantly increases the loading at the modulator input. An alternative approach ((Fig. 3(b)) is to first replace the distributed feedback paths, except for the first and last

paths, with feedforward paths [38], [39] without affecting the NTF. Then, to achieve an STF $= 1$, the input signal X needs to be added only to the outputs of the last two integrators, as shown by the dashed lines in Fig. 3(b). A further reduction in the input loading can be achieved ((Fig. 3(c)) by mapping the distributed-DAC-feedback modulator into a single-DAC-feedback structure without affecting the NTF. Then, to achieve an STF $= 1$, the input signal X needs to be added to the output of only the last integrator, as shown by the dashed path in Fig. 3(c). However, in this case, a weighted summation amplifier would be required at the quantizer input.

III. Design of the NTF and Modulator Stability

A. FIR NTFs

The simplest NTF, which can achieve a high SQNR for high-order $\Delta\Sigma$ modulators even at a low OSR, is a high-pass FIR function with L zeros at dc. For a given $\Delta\Sigma$ modulator of order L, the attainable SQNR can be further increased by shifting two complex-conjugate zeros of the NTF from dc to a frequency f_0 (within the signal band $[0, f_{\rm BW}]$) in a manner that minimizes the in-band quantization-noise power. For $L \geq 2$, this corresponds to

$$\text{NTF}(z) = (1 - z^{-1})^{L-2}(1 - \delta z^{-1} + z^{-2}) \tag{6}$$

where $\delta \equiv 2\cos(2\pi f_0/f_S)$, and results in the high-pass NTF characteristic having a notch at frequency f_0. Assuming additive white quantization noise and a brick-wall decimation filter, the optimal placement of the complex-conjugate zeros of NTF(z) is at approximately $f_0 = \sqrt{(2L-3)/(2L-1)}f_{\rm BW}$ and results in

$$\text{SQNR} = \frac{3}{2}\pi A_{\rm OL}^2(2^B - 1)^2\left(\frac{\text{OSR}}{\pi}\right)^{2L+1}(2L+1)(L-0.5)^2 \tag{7}$$

where $A_{\rm OL} = \|x\|_\infty/V_{\rm ref}$ is the quantizer overload ratio, $\|x\|_\infty = \max[|x(n)|]$ is the maximum amplitude of the input sine-wave signal X, and $V_{\rm ref}$ is the quantizer's reference voltage (full-scale range/2). This corresponds to a factor of $(L-0.5)^2$ improvement in SQNR relative to when all zeros of NTF(z) are at dc. (For example, with $L = 4$, $f_0 = 0.845 f_{\rm BW}$ results in an 11-dB SQNR improvement relative to $f_0 = 0$). Therefore, compared to spreading all the zeros of NTF(z) across the signal band as in [40], shifting only one pair of complex-conjugate zeros closer to $f_{\rm BW}$ still results (independently of OSR) in a substantial gain in SQNR, while requiring a much simpler circuit implementation as described in Section IV. Hence, this technique is particularly attractive for broad-band applications where the OSR is inherently low. In practice, the position f_0 of the notch in the high-pass NTF characteristic should be optimized taking into account the nonideal frequency response of the decimation filter. In general, simulations show that the SQNR sensitivity to the optimal f_0 is inherently low [37].

The FIR NTF in (6) results in an STF in (2) with a gain $|\text{STF}|$ of approximately[2] unity within the signal band but with a high-pass characteristic. Therefore, in addition to the advantages discussed in Section II, a flat unity-gain STF (i.e., $|\text{STF}| = 1$ over all frequencies) is further desirable in the case of an FIR NTF because: 1) it relaxes the requirements on the anti-aliasing filter preceding the $\Delta\Sigma$ modulator and 2) it enhances stability of the $\Delta\Sigma$ modulator by reducing the out-of-band spectral components in the quantizer's input signal (due to electronic noise, and when the modulator is driven by large transient signals with significant out-of-band energy), which may otherwise overload the quantizer.

[2]For OSR ≥ 8, $-0.3\text{dB} \leq |\text{STF}| \leq 0.3\text{dB}$ within $[0, f_{\rm BW}]$.

B. Stability of Multibit $\Delta\Sigma$ Modulators

Consider the multibit $\Delta\Sigma$ modulator modeled in Fig. 1. Assuming an STF $= 1$ and that the initial conditions of the $\Delta\Sigma$ modulator are such that the B-bit quantizer was not overloaded at any time before time 0, a sufficient condition to guarantee that the quantizer will never overload and, hence, ensure stability of the $\Delta\Sigma$ modulator [41], can be stated as

$$A_{\rm OL} \leq 1 - \frac{\|\text{ntf}\|_1 - 2}{2^B - 1} \tag{8}$$

where $\|\text{ntf}\|_1$ is the 1-norm of the impulse sequence ntf(n) for the noise transfer function NTF(z). For the Lth-order FIR NTF in (6) we have

$$\|\text{ntf}\|_1 \equiv \sum_{n=0}^{\infty}|\text{ntf}(n)| = (2+\delta)2^{L-2}. \tag{9}$$

Furthermore, in order to preserve stability in an actual circuit implementation of the $\Delta\Sigma$ modulator, it is usually necessary to: 1) scale the modulator coefficients in order to ensure that the peak outputs of the loop-filter integrators are within the bounds dictated by the opamp saturation voltages (i.e., perform dynamic-range scaling) and 2) consider the combined effects of the nonlinear opamp gains and the modulator coefficient variations when determining $\|\text{ntf}\|_1$ and the corresponding maximum stable input range. These nonidealities can cause $\|\text{ntf}\|_1$ to increase and, hence, cause the modulator to become unstable, especially when designing for an aggressive NTF.

The stability test in (8) clearly reveals that, with proper design, stability is not a limitation to a high-order multibit $\Delta\Sigma$ modulator with an FIR NTF. In general, this test leads to a conservative upper bound on the maximum stable input [40] because its derivation does not account for the correlation between successive quantization errors and for the dependence of these errors on the modulator input signal. Higher order ($L \geq 3$) multibit $\Delta\Sigma$ modulators tend to decorrelate successive quantization errors [1], [42] and, hence, this stability test appears to be less conservative in these cases.

IV. $\Delta\Sigma$ Modulators With FIR NTFs and Unity-Gain STFs

In this section, a multibit $\Delta\Sigma$ modulator with a single-stage single-DAC-feedback architecture is proposed to realize an FIR NTF and a unity-gain STF. With a single-stage architecture rather than a cascaded or MASH topology [1], the $\Delta\Sigma$ modulator is much less sensitive to the finite dc gains of the opamps and, hence, is more suitable for low-power design

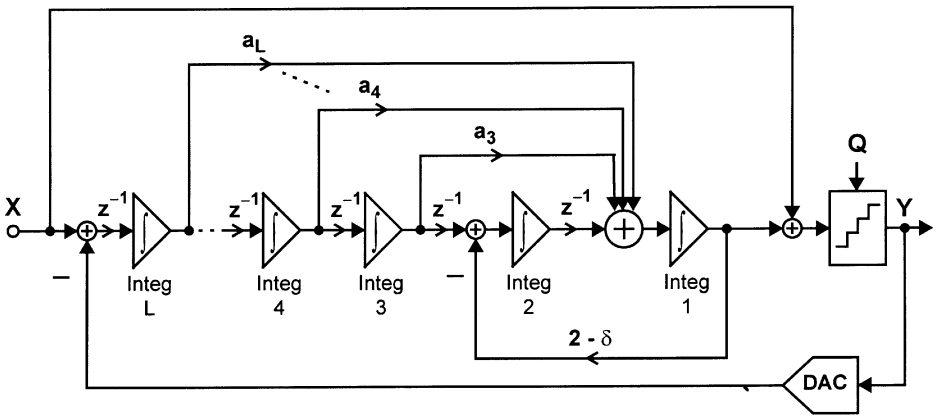

Fig. 4. Proposed $\Delta\Sigma$ modulator of order L ($L \geq 3$). The feedforward coefficients a_i ($i = 3, \ldots, L$) needed to realize the FIR NTF in (6) are given in Table II. Here, $\int \equiv 1/(1 - z^{-1})$.

TABLE II
FEEDFORWARD COEFFICIENTS $a_i (i = 3, \ldots, L)$ NEEDED TO REALIZE THE LTH-ORDER ($L \geq 3$) FIR NTF IN (6) USING THE PROPOSED $\Delta\Sigma$ MODULATOR IN FIG. 4

L	a_3	a_4	a_5
3	$\delta + 1$		
4	2 and $2\,z^{-1}$	$\delta + 2$	
5	5	5	$\delta + 3$

For $L = 4$, path a_3 consists of two parallel paths: a non-delaying path with coefficient 2 and a delaying path with coefficient $2\,z^{-1}$.

in scaled CMOS technologies. Furthermore, a single DAC feedback rather than a distributed DAC feedback within the multibit $\Delta\Sigma$ modulator significantly reduces the complexity of implementing the analog and DAC-linearization circuits, the chip area, and the power dissipation, especially when bootstrapped switches are needed in low-voltage designs [24].

A. Proposed $\Delta\Sigma$ Modulator

To implement an FIR NTF (with $L \geq 3$) and a unity-gain STF, the multibit $\Delta\Sigma$ modulator architecture shown in Fig. 4 is proposed [43]. This mathematical model can be directly mapped to an SC circuit [35]. The modulator coefficients needed to realize the FIR NTF in (6) are given in Table II. Except for the finite-zero loop-gain parameter δ, these coefficients are independent of e OSR and f_S. The implementation of the complex-conjugate zeros in the FIR NTF is achieved by one additional local feedback around the last two integrators in the loop filter (thereby forming a resonator) and, hence, requires very little analog circuitry. Although integrators with both delaying and nondelaying paths are required to implement an FIR NTF, the high-frequency settling properties of the proposed architecture is enhanced by designing the $\Delta\Sigma$ modulator with no delay-free loops and by interconnecting the loop-filter integrators such that the worst-case settling when $\delta = 2$ corresponds to two opamps settling in series.

B. Traditional Feedforward $\Delta\Sigma$ Modulator

Alternatively, an FIR NTF can also be implemented using the traditional feedforward $\Delta\Sigma$ modulator structure [10], [14], [44] as shown in Fig. 5. The corresponding modulator coefficients needed to realize the FIR NTF in (6) are given in Table III. Note that the $\Delta\Sigma$ modulator proposed in [31] falls as a special case of the feedforward $\Delta\Sigma$ modulator in Fig. 5 when $L = 2$ and $f_0 = 0$ ($\delta = 2$).

The proposed $\Delta\Sigma$ modulator in Fig. 4 offers the following advantages over the traditional $\Delta\Sigma$ modulator in Fig. 5.

1) The circuit complexity is reduced by not requiring a weighted summation amplifier before the quantizer. In the proposed $\Delta\Sigma$ modulator (Fig. 4), the summation of the signals in the feedforward paths is performed within the last integrator stage of the loop filter.
2) The sensitivity of the $\Delta\Sigma$ modulator to process variations in the modulator coefficients is significantly reduced, as demonstrated by the simulation results in Section IV-C. This improved robustness to coefficient variations could be attributed to the reduced number of feedforward paths in the proposed $\Delta\Sigma$ modulator, as every feedforward path corresponds to a cancellation in the NTF and STF of the modulator.
3) After proper dynamic range scaling, the modulator coefficients needed to realize an FIR NTF using the traditional feedforward structure (Fig. 5) have larger ratios compared to those in the proposed architecture (Fig. 4), thereby introducing large capacitor-ratio spreads in SC implementations. For example, in a fifth-order modulator with an OSR $= 8$ and an optimal zero placement, the largest coefficient ratio is 5 in the proposed architecture (Table II) while the coefficient ratio b_5/b_1 is 390.5 in the traditional topology (Table III).

C. Behavioral Simulation Results

The $\Delta\Sigma$ modulators in Figs. 4 and 5 were simulated in SIMULINK. The gain and phase errors in the transfer function of the loop-filter integrators, due to the nonlinear dc gains of the opamps, were modeled as described in [45]. The opamps were assumed to have nonlinear dc gains corresponding to an input–output transfer curve in the form of a hyperbolic tangent with a maximum dc gain of A_{opamp} and an output saturation voltage of $V_{O,\text{sat}}$. A sine-wave signal with an amplitude $\|x\|_\infty$ and a frequency $f_S/(2\ \text{OSR})$ was applied at the input. A

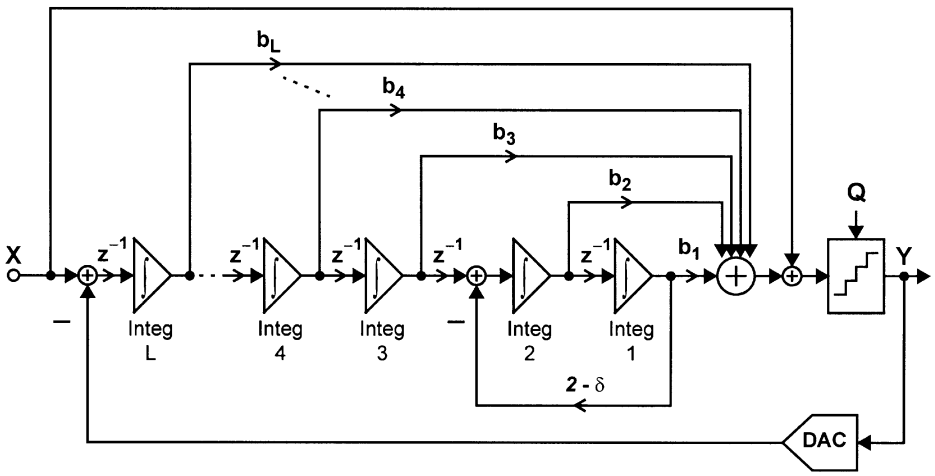

Fig. 5. Traditional feedforward $\Delta\Sigma$ modulator of order L ($L \geq 2$). The feedforward coefficients b_i ($i = 1, \ldots, L$) needed to realize the FIR NTF in (6) are given in Table III. Here, $\int \equiv 1/(1 - z^{-1})$.

TABLE III
FEEDFORWARD COEFFICIENTS b_i ($i = 1, \ldots, L$) NEEDED TO REALIZE THE LTH-ORDER ($L \geq 2$) FIR NTF IN (6) USING THE TRADITIONAL $\Delta\Sigma$ MODULATOR IN FIG. 5

L	b_1	b_2	b_3	b_4	b_5
2	δ - 1	δ			
3	δ^2 - δ - 1	δ^2 - 1	δ + 1		
4	δ^3 - δ^2 - 2 δ + 1	δ^3 - 2 δ	δ^2 + δ	δ + 2	
5	δ^4 - δ^3 - 3 δ^2 + 2δ + 1	δ^4 - 3 δ^2 + 1	δ^3 + δ^2 - δ	δ^2 + 2 δ + 2	δ + 3

sampling frequency of $f_S = 64$ MHz was used. An opamp saturation voltage of $V_{O,\text{sat}} = 1.2\|x\|_\infty$ was assumed and dynamic range scaling was performed to ensure that the peak outputs of the loop-filter integrators were at approximately $\|x\|_\infty/2$. The SNDR values reported in this paper correspond to the minimum SNDR values found over 100 simulations in which each modulator coefficient is assumed to have a uniformly-distributed random error in the range $\pm e_{\text{coeff}}$. The multibit DAC was assumed to be ideal in these simulations.

Fig. 6 shows the SNDR versus A_{opamp} of the proposed third-order modulator (with OSR $= 16$, $B = 5$ bits, and $A_{\text{OL}} = 0.75$) for $e_{\text{coeff}} = 0$ and 2%. Accordingly, the proposed $\Delta\Sigma$ modulator can achieve a high resolution (SNDR > 14 bits) using opamps with only moderate dc gains (150 V/V). Figs. 7 and 8 show the SNDR versus e_{coeff} of, respectively, a fourth-order modulator (with OSR $= 8$, $B = 6$ bits, and $A_{\text{OL}} = 0.75$) and a fifth-order modulator (with OSR $= 8$, $B = 6$ bits, and $A_{\text{OL}} = 0.5$) for various A_{opamp}. Therefore, as shown in Figs. 7(a) and 8(a), the traditional $\Delta\Sigma$ modulator can tolerate (in terms of stability) a maximum variation in the modulator coefficients of 0.75% and 0.2% for the fourth- and fifth-order modulators, respectively. However, as shown in Figs. 7(b) and 8(b), when the proposed $\Delta\Sigma$ modulator was simulated under identical conditions (including comparable integrator output voltages), the range of e_{coeff} that guaranteed a stable modulator increased to 2% and 0.5% for the fourth- and fifth-order modulators, respectively.

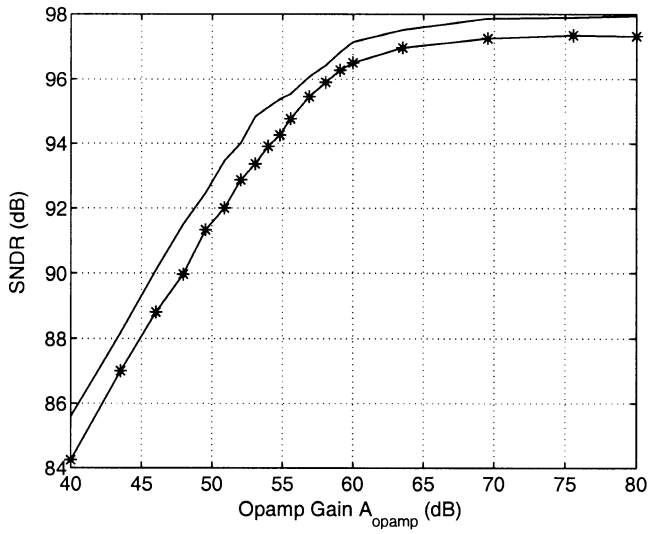

Fig. 6. SNDR versus A_{opamp} for a third-order $\Delta\Sigma$ modulator (with OSR $= 16$, $B = 5$ bits, and $A_{\text{OL}} = 0.75$) using the proposed architecture in Fig. 4. Here, —: $e_{\text{coeff}} = 0$; $-*-$: $e_{\text{coeff}} = 2\%$.

V. LINEARITY ENHANCEMENT OF MULTIBIT DACS

The linearity of a multibit $\Delta\Sigma$ modulator is limited by that of its internal multibit DAC because errors due to nonidealities in the feedback DAC add directly to the input signal and, therefore, are not shaped by the $\Delta\Sigma$ loop. High DAC linearity requires precise matching of the DAC unit elements. Rather than using special fabrication processes or laser trimmed components to improve the DAC element matching, two signal-processing strategies have been developed to enhance the linearity of multibit $\Delta\Sigma$ modulators due to DAC element mismatch [1]: 1) dynamic element matching (DEM) [33], [34] and 2) calibration/correction using analog [46], [47], digital [48], or mixed-mode [49] schemes. A combination of DEM and digital correction has also been proposed in [50] and [51].

A. DWA

Compared to DEM techniques such as data weighted averaging (DWA) [25], background calibration schemes are more

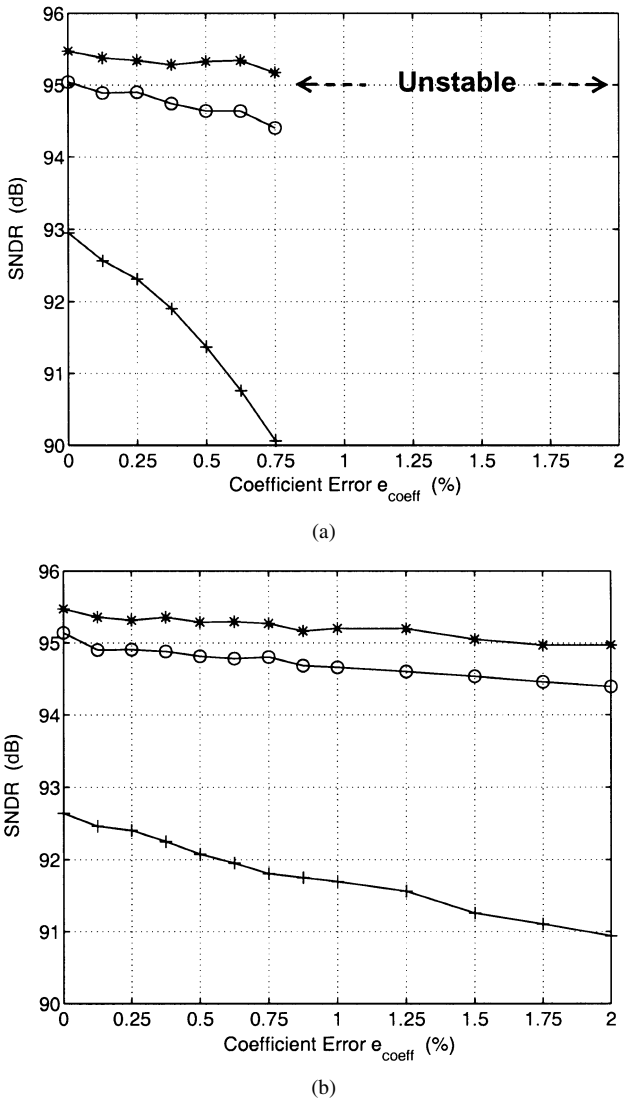

Fig. 7. SNDR versus e_{coeff} for a fourth-order $\Delta\Sigma$ modulator (with OSR $= 8$, $B = 6$ bits, and $A_{\mathrm{OL}} = 0.75$) using: (a) the traditional topology in Fig. 5 and (b) the proposed architecture in Fig. 4. Here, $-*-$: ideal opamp; $-o-$: $A_{\mathrm{opamp}} = 60$ dB; $-+-$: $A_{\mathrm{opamp}} = 50$ dB.

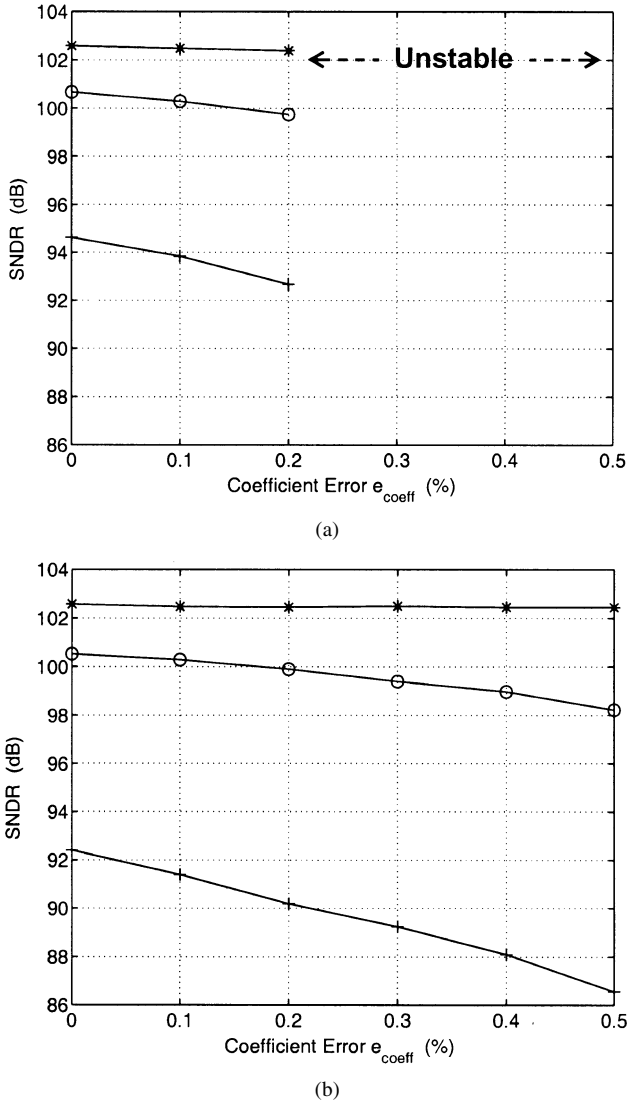

Fig. 8. SNDR versus e_{coeff} for a fifth-order $\Delta\Sigma$ modulator (with OSR $= 8$, $B = 6$ bits, and $A_{\mathrm{OL}} = 0.5$) using: (a) the traditional topology in Fig. 5 and (b) the proposed architecture in Fig. 4. Here, $-*-$: ideal opamp; $-o-$: $A_{\mathrm{opamp}} = 60$ dB; $-+-$: $A_{\mathrm{opamp}} = 50$ dB.

expensive to implement in terms of system design complexity, hardware requirement, and power consumption. Indeed, all high-speed high-resolution $\Delta\Sigma$ ADCs with multibit $\Delta\Sigma$ modulators reported in Table I rely (except [3]) on DWA or a modified version of DWA in order to linearize their internal multibit DACs. In such high-speed $\Delta\Sigma$ modulators, the complexity of the DEM algorithm becomes a concern because the delay introduced by the DEM selection logic in the $\Delta\Sigma$ feedback loop (Fig. 1) can limit the maximum achievable clock speed for the $\Delta\Sigma$ modulator. In that respect, DWA is a highly practical DEM technique to implement, especially when the number of DAC elements is large.

In DWA, the DAC unit elements participating in the D/A conversion are selected sequentially from the DAC array, beginning with the next available unused element. A pointer, hereafter called the index pointer ptr, directs the element-selection process. Through such rotational element-selection process, DWA achieves first-order high-pass shaping of the DAC mismatch errors [33], [52]. However, it can also introduce in-band signal-dependent tones in the modulator's output spectrum ((as depicted in Fig. 9(a)) [25], [53].

B. Tone Behavior of DWA

In DWA, because the same set of DAC elements is used cyclically and repeatedly under the guide of a single pointer [53], the element mismatch errors translate to tones at the DAC output when the DAC input codes have a periodic pattern. These tones add directly to the modulator's input signal and appear unshaped at the modulator output. Out-of-band tones generated by DWA may then fold back to the signal band due to modulation by the modulator's output waveform. The tone behavior of DWA depends on the number of DAC elements, the pattern of the DAC element mismatch, the amplitude and frequency of the modulator's input signal, and various circuit parameters which affect the modulator's output waveform [26], [53]. For example, consider the case when the consecutive input codes to the M-element DAC in Fig. 1 have the same value Y_{DAC} (i.e., $y(n) =$

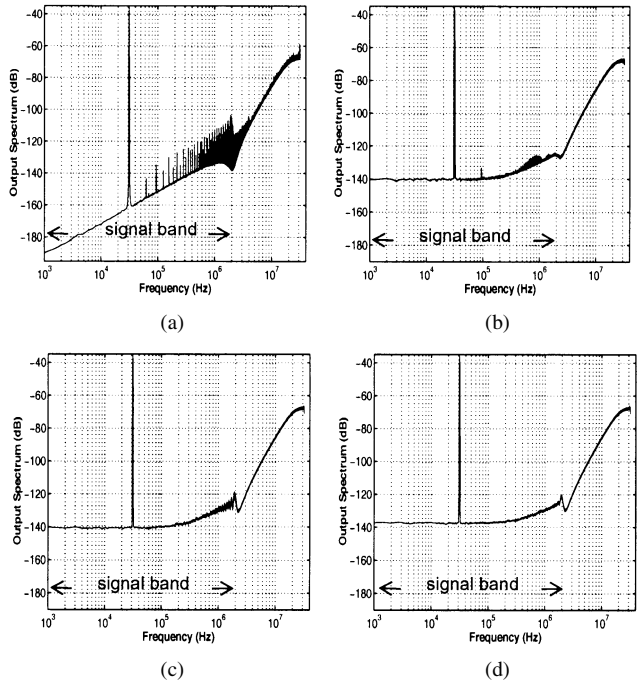

Fig. 9. Output spectrum of the $\Delta\Sigma$ modulator using: (a) DWA [25], (b) P-DWA [12], (c) Pseudo DWA with $n_{\rm inv} = 128$, and (d) Pseudo DWA with $n_{\rm inv} = 64$. (Input signal: -30 dBFS at $f_S/2048$.)

$Y_{\rm DAC}$). As is common, define the mismatch error ε_i in the DAC unit element U_i $(i = 0, \ldots, M-1)$ as

$$U_i \equiv U_{\rm mean}(1+\varepsilon_i), \text{ where } U_{\rm mean} \equiv \frac{1}{M}\sum_{i=0}^{M-1} U_i. \qquad (10)$$

The DWA algorithm will select DAC unit elements in a rotational manner, making a complete rotation (with the index pointer returning to its exact starting point) every M/r clock cycles, where r is the greatest common divisor of $Y_{\rm DAC}$ and M. As a result, the DAC mismatch noise will be a periodic sequence

$$\left\{ \sum_{i=0}^{Y_{\rm DAC}-1} \varepsilon_i, \sum_{i=Y_{\rm DAC}}^{2Y_{\rm DAC}-1} \varepsilon_i, \ldots, \sum_{i=M-Y_{\rm DAC}}^{M-1} \varepsilon_i, \sum_{i=0}^{Y_{\rm DAC}-1} \varepsilon_i, \ldots \right\} \qquad (11)$$

of period MT_S/r (where $T_S = 1/f_S$), and its power spectrum will take the form of tones at frequencies [26]

$$f_{\rm tone} = k\frac{r}{M} f_S, \qquad k = 1, 2, \ldots \qquad (12)$$

Thus, in general, for an M-element DAC, the lowest tone frequency can be at f_S/M with DWA. If the maximum possible input frequency to the $\Delta\Sigma$ modulator is $f_{\rm BW} = f_S/(2{\rm OSR})$, then the constraint that the kth harmonic of the modulator's input signal does not fall back into the signal bandwidth after being modulated by the DWA tone at f_S/M requires that [53]

$$\frac{f_S}{M} - k f_{\rm BW} > f_{\rm BW} \Leftrightarrow {\rm OSR} > \left(\frac{1+k}{2}\right) M. \qquad (13)$$

In summary, the tone problem of DWA degrades the SFDR of the $\Delta\Sigma$ modulator and can preclude using DWA at a low OSR, especially when the number of DAC elements (quantization bits) is large. In the following, a simple technique will be proposed to solve this problem.

VI. Pseudo DWA

A. Pseudo DWA Algorithm

Consider an M-element DAC with input code $y(n)$. In conventional DWA, the DAC unit elements selected at time n are those from $ptr(n)$ to $[ptr(n)+y(n)-1] \bmod M$, by increasing order. The index pointer $ptr(n)$ (i.e., the address of the next available unused element) is stored in a digital register. Every clock cycle, the index pointer is incremented modulus M by the DAC input code $y(n)$

$$ptr(n+1) = [ptr(n) + y(n)] \bmod M,$$
$$0 \le ptr(n) \le M-1. \qquad (14)$$

The technique proposed in this paper, called Pseudo DWA, modifies the DWA scheme by periodically inverting the LSB of the DAC input code $y(n)$ used to update the index pointer in (14)[29]. Let $\boldsymbol{n_{\rm inv}}$ denote the number of clock cycles between each such LSB inversion. Then, the element-selection process in Pseudo DWA is essentially similar to conventional DWA except that, every $n_{\rm inv}$ clock cycles, a DAC element is either reselected or skipped depending on whether the previous DAC input code was, respectively, odd or even. For example, assume that $ptr(n+1)$ has a value P in (14). If the corresponding $y(n)$ is even, its LSB inversion will increase $ptr(n+1)$ by 1. As a result, on the next clock cycle (i.e., at time $n+1$), the Pseudo DWA algorithm will select DAC elements starting with element U_{P+1} (i.e., element U_P is skipped). Alternatively, if the corresponding $y(n)$ is odd, its LSB inversion will decrement $ptr(n+1)$ by 1. As a result, on the next clock cycle, the Pseudo DWA algorithm will select DAC elements starting with element U_{P-1} (i.e., element U_{P-1} is reselected). This simple modification to DWA breaks the cyclic nature of the element-selection process and, hence, reduces the tone behavior.

B. Performance of Pseudo DWA

The Pseudo DWA algorithm is implemented in a third-order $\Delta\Sigma$ ADC with a 5-bit quantizer, a 31-element DAC, and a 16 $\times$ OSR. The $\Delta\Sigma$ ADC is based on the proposed $\Delta\Sigma$ modulator (Fig. 4), with the NTF having one zero at dc and two complex-conjugate zeros at the signal-band edge $f_{\rm BW}$. The results reported in this paper correspond to the average of 100 SIMULINK simulations assuming a random DAC element mismatch of 0.5% (1σ). These behavioral simulations account for the nonlinear dc gains of the opamps in the loop-filter integrators as described in Section IV-C, with $A_{\rm opmap} = 150$ V/V. Furthermore, these simulations include the quantization noise and the DAC mismatch noise, but no other analog device noise. Since simulations with an ideal DAC showed no obvious in-band tones in the output spectrum of the $\Delta\Sigma$ modulator, it can be assumed that, with a nonideal DAC, any in-band tones are generated by the DAC element-mismatch errors.

In Pseudo DWA, the choice of $n_{\rm inv}$ is a compromise between linearity and resolution. If $n_{\rm inv}$ is too large ($n_{\rm inv} = \infty$ corresponds to conventional DWA), the signal-dependent tones will

TABLE IV
ACHIEVABLE PEAK SNDR USING VARIOUS DWA SCHEMES IN A THIRD-ORDER $\Delta\Sigma$ MODULATOR WITH OSR $= 16$, $B = 5$ BITS, AND $M = 31$ ELEMENTS. A RANDOM DAC-ELEMENT MISMATCH OF 0.5% IS ASSUMED. (INPUT SIGNAL: -2 dBFS AT $f_S/2048$)

DAC Linearization	Peak SNDR (dB)
Ideal DAC	92.8
No DWA	60.4
DWA [25]	90.9
Pseudo DWA, $n_{inv} = 128$	89.9
Pseudo DWA, $n_{inv} = 64$	89.1
P-DWA [12]	89.7
Bi-DWA [8]	85.8
RnDWA [28]	83.2
IDWA [26]	82.0

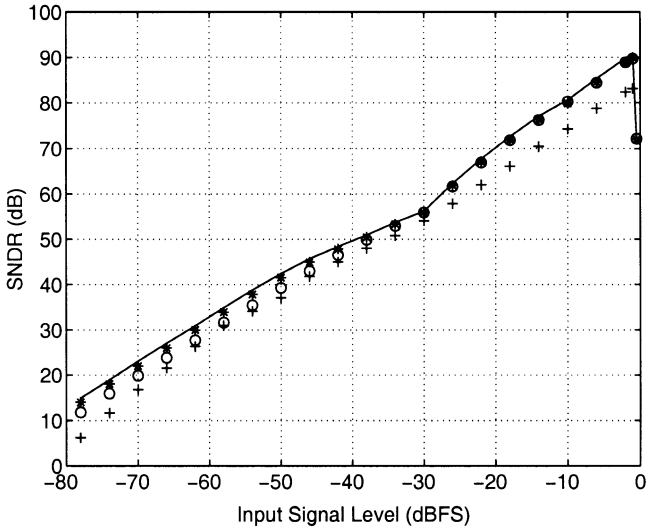

Fig. 10. SNDR versus input signal levels when using: — DWA [25]; –∗– Pseudo DWA; –o– P-DWA [12]; –+– RnDWA [28] with an ideal implementation.

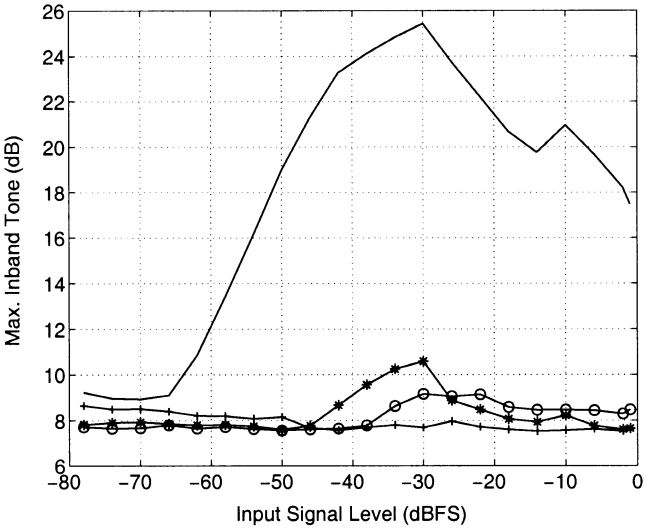

Fig. 11. Maximum in-band tone versus input signal levels when using: — DWA [25]; –∗– Pseudo DWA; –o– P-DWA [12]; –+– RnDWA [28] with an ideal implementation.

not be eliminated. If $n_{\rm inv}$ is too small, different DAC elements will be used at significantly different rates. Simulations show that this increases the inband mismatch noise and degrades the SNDR. Deriving an analytical expression for the optimum value of $n_{\rm inv}$ is rather complex because the DWA tone behavior depends on the various circuit parameters which affect the modulator output waveform (as discussed in Section V). However, for a given $\Delta\Sigma$ modulator, simple behavioral simulations can be easily used to find the appropriate value of $n_{\rm inv}$. For the $\Delta\Sigma$ modulator described above, the simulation results presented below indicate that an $n_{\rm inv}$ between 64 and 128 is a good choice for preventing the DWA tones without sacrificing the SNDR. These results have also been verified experimentally in [24].

Fig. 9(a) shows strong in-band tones in the output spectrum of the $\Delta\Sigma$ modulator when using DWA. When using Pseudo DWA and $n_{\rm inv} = 128$ (Fig. 9(c)) or $n_{\rm inv} = 64$ (Fig. 9(d)), these tones are smoothed in all frequencies and no notable tones are present in the signal band. This is accompanied with some increase in the inband noise. However, as depicted in Fig. 10, the degradation in SNDR compared to DWA is within 1 dB (for $n_{\rm inv} = 128$) over the full range of input signal levels. This implies that, if the DAC mismatch noise floor is below the overall noise floor of the ADC, it is beneficial to use Pseudo DWA and improve the SFDR.

C. Comparison of Pseudo DWA To Other DWA Schemes

A number of techniques have been proposed to solve the tone problem in DWA. These techniques can be classified into four categories: 1) Dithering [25]; 2) Incremental DWA (IDWA) [14], [26]; 3) DWA with multiple data-directed index pointers, as in Bi-Directional DWA (Bi-DWA) [8] and Partitioned DWA (P-DWA) [12]; 4) DWA with randomized index pointer, as in Rotated DWA (RDWA) [19], [27], Randomized DWA (RnDWA) [23], [28], and Pseudo DWA [24], [29]. A summary description of these techniques is presented in [29].

Table IV compares the peak SNDR when using the above techniques for DWA tone reduction. In classical DWA, the efficiency of the DAC mismatch errors averaging to zero is determined by the rate of using each DAC unit element [25]. The use of an extra DAC element in IDWA, the switching between separate pointers in Bi-DWA, and the frequent jumps in the index pointer in RnDWA, reduce this rate and degrade the SNDR. For P-DWA, Fig. 10 shows that the degradation in SNDR compared to DWA is within 1.2 dB for input signal levels above -40 dB, but is over 3 dB for lower levels. Furthermore, as shown in Fig. 9(b), P-DWA still generates notable signal-dependent tones within the signal band.

Fig. 11 shows the maximum in-band tone relative to the average tone power. Compared to DWA, reductions of about 15,

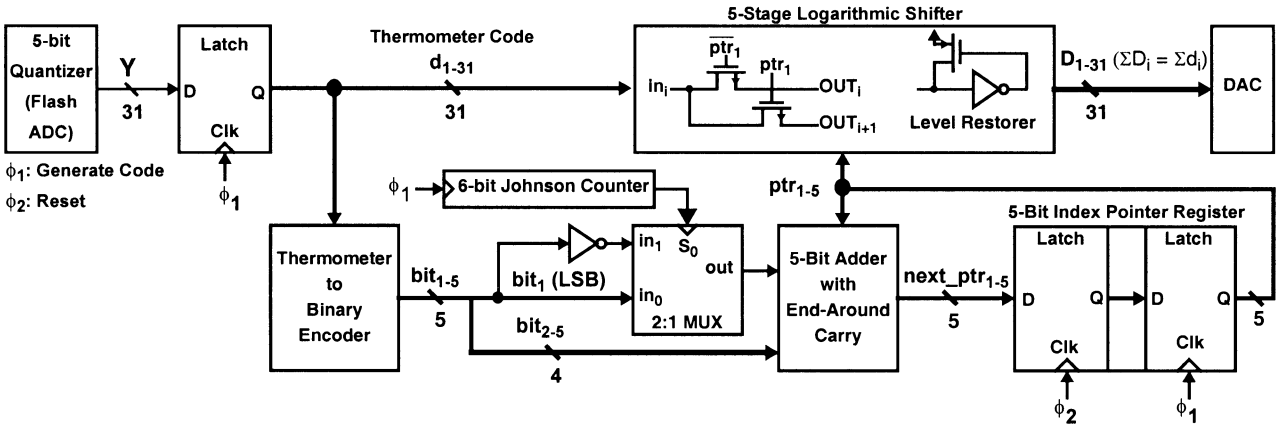

Fig. 12. Implementation of the Pseudo DWA algorithm.

16, and 18 dB in the maximum in-band tone are achieved using Pseudo DWA, P-DWA, and RnDWA (with an ideal implementation [29]), respectively. Note that, in general, a modified DWA technique cannot completely eliminate the in-band DWA tones and achieve a smooth DAC noise floor over all input signal levels, unless a perfectly random component is introduced in the DAC element-selection process (for example, in an ideal implementation of a randomized DWA technique [29]). However, assuming a 0.5% DAC-element mismatch in the $\Delta\Sigma$ ADC described above, behavioral simulations show that the largest in-band tone with Pseudo DWA is well below the level of the kT/C noise floor for the ADC. Thus, such in-band tone will not be visible in the ADC output spectrum and will not degrade its performance.

D. Implementation of Pseudo DWA

The implementation of any DEM algorithm is critical for the achievable clock speed because the DEM block (element-selection logic in Fig. 1) adds extra delay in the $\Delta\Sigma$ feedback loop. In an SC implementation of a $\Delta\Sigma$ modulator, the B-bit quantizer is typically realized using as an M-level flash ADC and a two-phase nonoverlapping clock is used. Only half a clock period is available for the thermometer output code of the flash ADC to be generated, processed by the DEM block, and D/A converted by the DAC. Therefore, the DEM logic must be optimized for minimal delay in the $\Delta\Sigma$ feedback path [9].

Fig. 12 shows the implementation of the Pseudo DWA algorithm (with $n_{\text{inv}} = 64$) in a $\Delta\Sigma$ ADC with a 5-bit quantizer and a 31-element DAC [24]. Here, the 5-bit quantizer is realized using a flash ADC with a 31-digit thermometer output-code d_{1-31}. A five-stage logarithmic shifter in the $\Delta\Sigma$ feedback path provides the rotation of the 31-digit code d_{1-31} as required by the Pseudo DWA algorithm, thereby generating an equivalent 31-digit code D_{1-31} which selects the DAC unit-elements (Fig. 1). The 5-bit control signal of the shifter corresponds to the index pointer ptr_{1-5} and should be stable during phase ϕ_1 when the thermometer code ripples through the shifter. The shifter is implemented using only NMOS transistors, with level restorers after the third and fifth stages to achieve minimal delay. The index pointer ptr_{1-5} is updated every clock cycle as follows: 1) an encoder converts the 31-digit thermometer output-code d_{1-31} to a 5-bit binary output-code bit_{1-5}; 2) a 5-bit adder, with end-around carry, increments the index pointer ptr_{1-5} modulus 31 by the output code bit_{1-5} and generates the next index pointer $next\_ptr_{1-5}$ (i.e., the index pointer to be used at the next ϕ_1); 3) every 64 clock cycles ($n_{\text{inv}} = 64$), the LSB of the quantizer output code (bit_1) is inverted before updating the index-pointer register. A 6-bit Johnson counter and a 2:1 mux are used to control the timing of the LSB inversion. This is **the only additional hardware** required to implement Pseudo DWA instead of DWA. Accordingly, Pseudo DWA adds no extra delay in the critical feedback path (phase ϕ_1) of the $\Delta\Sigma$ loop.

VII. Conclusion

Techniques to modify single-feedback and distributed-feedback $\Delta\Sigma$ modulator topologies in order to achieve a unity-gain STF without affecting the NTF were described. Such an STF is generally more desirable than any other STF characteristic as it reduces the modulator sensitivity to integrator nonidealities and, hence, helps minimizing the power dissipation. Next, a multibit $\Delta\Sigma$ modulator was proposed to realize high-order FIR NTFs (with a pair of complex-conjugate zeros optimally placed across the signal band) to achieve high SQNRs at low OSRs. Its circuit implementation is simpler than traditional $\Delta\Sigma$ modulator structures and simulations confirm its reduced sensitivity to integrator nonlinearities and its improved robustness to coefficient variations. Thus, the proposed $\Delta\Sigma$ modulator is particularly suitable for realizing broadband low-distortion ADCs. Finally, Pseudo DWA was proposed to remedy the tone behavior of DWA without sacrificing the SNDR. It implementation adds no extra delay in the $\Delta\Sigma$ feedback loop and requires only minimal additional digital-signal-processing. Simulations confirm the improved accuracy achievable by Pseudo DWA at low OSRs.

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