Digital Background Calibration of Interstage-Gain and Capacitor-Mismatch Errors in Pipelined ADCs

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***Abstract*— Two digital background-calibration techniques are proposed to correct for linearity errors due to capacitor mismatches and opamp nonidealities in the pipelined stages of a pipelined analog-to-digital converters (ADC): *1) Capacitor-Mismatch Calibration*: The feedback capacitor is randomly swapped with the sampling capacitor(s) in the multiplying digital-to-analog converter (MDAC) of each pipeline stage, during the normal ADC operation. The capacitor-mismatch errors in all stages are then concurrently calibrated in the digital domain. The proposed technique is applicable to both 1.5- and multi-bit MDACs. In a 13-bit pipelined ADC with 0.25% (1σ) capacitor-mismatch errors, it improves the SNDR from 10 to 12.5 bits and the SFDR from 65 to 95 dB. *2) Interstage-Gain Calibration*: Gain errors due to opamp nonidealities in the MDAC of each pipeline stage are modeled using a 4th-order Taylor series expansion of the opamp output and are digitally calibrated. Compared to previously-reported methods for zero- and 2nd-order gain-calibration, the proposed technique for 4th-order gain-calibration reduces the opamp dc gains required to achieve a 13-bit SNDR in a 14-bit pipelined ADC by 22 dB and 9 dB, respectively. Behavioral simulation results are presented.**

I. INTRODUCTION

The linearity of a pipelined analog-to-digital converter (ADC) is primarily degraded by the linearity errors in its pipeline stages. Consider a typical pipeline stage with digital redundancy [1], as depicted in Fig. 1. In its switched-capacitor circuit implementation, the primary sources of linearity errors are: a) the gain errors in its residue amplifier, due to operational-amplifier (opamp) nonidealities; and b) the nonlinearity in its digital-to-analog sub-converter (sub-DAC), due to capacitor-mismatch errors.

This paper proposes two independent techniques for digital background calibration of pipelined ADCs. The first technique is for capacitor-mismatch calibration and the second technique is for interstage-gain calibration. In these techniques, the measurement and correction of the capacitor-mismatch and gain errors in the pipeline stages of a pipelined ADC are performed: a) *fully digitally*, without requiring any additional high-precision analog circuits [2]; and b) *concurrently* in all pipeline stages during the normal ADC operation, without requiring any special calibration signal [3] to be injected at the input of the pipeline stages.

The proposed capacitor-mismatch calibration technique randomly swaps the feedback capacitor with the sampling capacitor(s) in the multiplying digital-to-analog converter (MDAC) of each pipeline stage in a pipelined ADC, in order to measure and correct for capacitor-mismatch errors. Other digital background calibration methods for capacitor-mismatch errors, which utilize capacitor shuffling or capacitor swapping to mitigate the linearity error due to capacitor mismatches in pipelined ADCs, have been suggested in [4,5,6,7]. However, the calibration method in [4] targets multi-bit pipeline stages only (with large digital circuits required to implement its capacitor-shuffling logic [8]), while the calibration method in [5] is only intended for single-bit pipeline stages. In [6], a DFCA (DAC-and-feedback-capacitor-averaging) technique spreads the signal harmonics, followed by a hardware-intensive MNC (mismatch-noise-cancellation) technique [7]. Hence, when using the DFCA technique, the spurious-free dynamic range (SFDR) of the ADC is improved, but not its signal-to-noise-and-distortion ratio (SNDR) because its noise floor is not decreased.

In this paper, the proposed capacitor-mismatch calibration technique improves both the SFDR and SNDR of pipelined ADCs with single- and multi-bit pipeline stages. Since the proposed technique utilizes relatively simple relations to estimate the capacitor mismatch error, only a small digital-circuit block is needed to implement its calibration logic.

The proposed interstage-gain calibration technique extends the calibration method in [9] to account for high-order opamp nonidealities and, hence, more accurately correct for the MDAC gain error in each pipeline stage of a pipelined ADC. This requires a relatively larger digital logic. However, as demonstrated by the simulation results in Section IV, a high-order gain calibration is critical for designing high-resolution pipelined ADCs (SNDR ≥ 13 bits) using opamps with low dc gains (≤ 55 dB). Hence, it is more suited for low-power designs, especially in nano-scale CMOS technologies. In these technologies, high dc gains for the opamps are difficult to achieve at low power, due to the low supply voltages and the poor intrinsic gains of the MOS transistors.

The paper outline is as follows: Digital background techniques are proposed in Sections II and III for the calibration of, respectively, capacitor-mismatch errors and interstage-gain errors in both single- and multi-bit MDACs of a pipelined ADC. Section IV describes example implementations of both techniques in a pipelined ADC and presents the simulation results.

II. CAPACITOR-MISMATCH CALIBRATION TECHNIQUE

A. *Digital Calibration of* 1-*Bit Pipeline Stages*

Consider the "capacitor-flip-over" MDAC in Fig. 2(a), which is widely utilized to realize 1-bit pipeline stages. Define the capacitor-mismatch error as

$$\delta C \equiv (C_S - C_F)/C_F \tag{1}$$

where C_S and C_F are the sampling and feedback capacitors, respectively. Assuming no gain errors due to opamp nonidealities, the MDAC residue (output) signal can then be expressed as

$$r = 2x\left(1+\frac{\delta C}{2}\right) - D_1(1+\delta C)V_{ref} \tag{2}$$

Here, the digit D_1 (i.e., the sub-ADC output of the pipeline stage in Fig. 1) is $+V_{ref}$ or $-V_{ref}$, depending on the input signal x. A unity reference voltage (V_{ref}=1) will be assumed for simplicity.

In the proposed capacitor-mismatch calibration technique, the roles of capacitors C_S and C_F are randomly interchanged (i.e., C_S and C_F are randomly swapped) during the hold clock-phase φ_2 in order to digitally measure the capacitor-mismatch error δC.

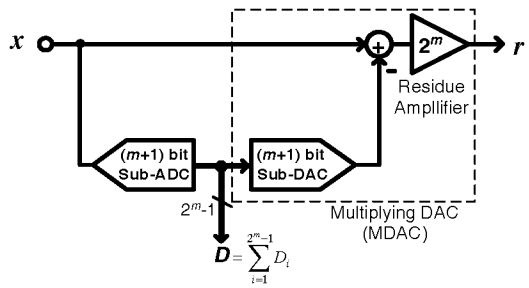

Fig. 1. A pipeline stage with an m-bit effective resolution and a 1-bit redundancy for digital error correction.

As depicted in Fig. 3, such capacitor swapping is achieved using a pseudo-random control signal N with a value of +1 (to connect C_F in feedback) or -1 (to connect C_S in feedback). Thus, when N=-1, the roles of C_F and C_S are interchanged and, hence, the value of δC must be interchanged with

$$\delta C\big|_{N=-1} = (C_F - C_S)/C_S = -(\delta C + \delta C^2) \approx -\delta C \tag{3}$$

in expression (2) for the MDAC residue signal r.

Accordingly, in general, the MDAC residue signal r can be expressed for both values of N as:

$$r = 2x\left(1 + N\frac{\delta C}{2}\right) - D_1\left(1 + N\,\delta C\right) \tag{4}$$

In the proposed calibration technique, the value of δC is estimated in the digital domain, as described below.

Let R denote the digital representation of the MDAC residue signal r in equation (4). Furthermore, assume that the value of r is digitized (by the subsequent pipeline stages in the pipelined ADC) as R, without any error. Then, using (4), the corrected value of R can be expressed as

$$\hat{R} = 2x\left(1 + N\frac{(\delta C - \hat{\delta C})}{2}\right) - D_1\left(1 + N\,(\delta C - \hat{\delta C})\right) \tag{5}$$

where $\hat{\delta C}$ denotes the estimated value of δC. To estimate the value of capacitor-mismatch error δC, assume that the pseudo-random control signal N has a zero mean value (i.e., both C_F and C_S are equally utilized as the feedback capacitor). Then, since N^2=1 and D^2=1 (for a 1-bit MDAC), defining

$$V_{\hat{R}ND} \equiv \hat{R}\,N\,D_1 \tag{6}$$

results in

$$V_{\hat{R}ND} = (xD_1 - 1)\left(\delta C - \hat{\delta C}\right) + (2xD_1 - 1)N \tag{7}$$

If the estimated value $\hat{\delta C}$ for the capacitor-mismatch error is equal to the actual value δC, then the average value of $V_{\hat{R}ND}$ will be zero (as N and x are independent and N has a zero mean value). Therefore, by starting with an initial value for $\hat{\delta C}$ and then utilizing $V_{\hat{R}ND}$ to iteratively update $\hat{\delta C}$ in the digital domain, the estimated value $\hat{\delta C}$ will converge to the actual value δC.

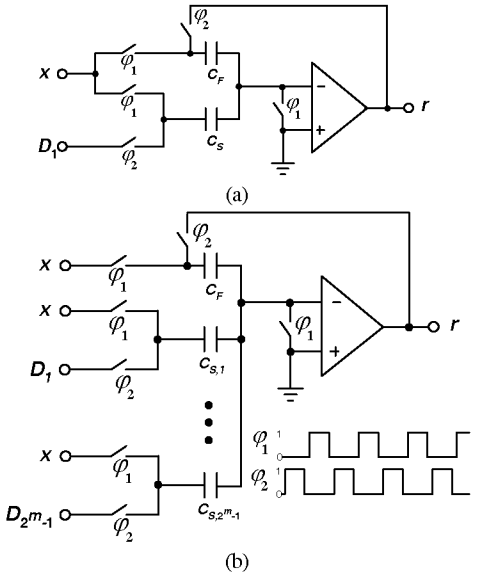

Fig. 2. Capacitor flip-over MDAC for:
(a) 1-bit or 1.5-bit pipeline stages; and (b) multi-bit pipeline stages.

Accordingly, $\hat{\delta C}$ can be iteratively updated in the digital domain using the iterative relation

$$\hat{\delta C}(n+1) = \hat{\delta C}(n) - \varepsilon V_{\hat{R}ND} \tag{8}$$

where n is the iteration index and ε is the update step size. Note that the factor (xD_1-1) in equation (7) is always negative (as, ideally, $|x|$<1 and D_1=sign(x)). Hence, the average value of $V_{\hat{R}ND}$ is positive/negative when $\hat{\delta C}$ is larger/smaller than δC. Therefore, the negative sign in the iterative relation (8) ensures that $\hat{\delta C}$ converges to δC. Furthermore, by decreasing the value of ε, the effect of input-signal interference in estimating δC is suppressed. However, for a given resolution, this increases the time required to estimate δC [10].

B. Digital Calibration of 1.5-bit Pipeline Stages

The MDAC in Fig. 2(a) is also widely utilized to realize 1.5-bit pipeline stages. In this case, the digit D_1 is ±1 or 0, depending on the input signal x (i.e., the sub-ADC output of the pipeline stage in Fig. 1). When D_1=0, $V_{\hat{R}ND}$ =0 and, hence, the iterative relation in (8) for the estimation of the capacitor-mismatch error δC is not affected. Therefore, the proposed calibration technique described above for a 1-bit pipeline stage (where D_1=±1) can be directly utilized in a 1.5-bit pipeline stage (where D_1=±1 or 0), as demonstrated by the simulation results in Section IV.

C. Digital Calibration of Multi-Bit Pipeline Stages

Consider the multi-bit MDAC in Fig. 2(b), which is widely utilized to realize pipeline stages with an m-bit effective resolution. Define the mismatch error in each sampling capacitor as

$$\delta C_k \equiv (C_{S,k} - C_F)/C_F, \qquad k = 1,...,2^m - 1 \tag{9}$$

where C_F is the feedback capacitor and $C_{S,k}$ are the sampling capacitors (k=1,...,2^m-1). Then, the MDAC residue (output) signal can be expressed as:

$$r = 2^m x\left(1 + \frac{1}{2^m}\sum_{i=1}^{2^m-1}\delta C_i\right) - \sum_{i=1}^{2^m-1} D_i\left(1 + \delta C_i\right)V_{ref} \tag{10}$$

Here, each digit D_k (k=1,...,2^m-1) is 0 or ±1, depending on the input signal x (i.e., the sub-ADC output of the pipeline stage in Fig. 1).

In the proposed capacitor-mismatch calibration technique, each capacitor $C_{S,k}$ is randomly swapped with capacitor C_F (i.e., their roles are interchanged) during the hold clock-phase φ_2 to measure the corresponding capacitor-mismatch error δC_k. When this is performed,

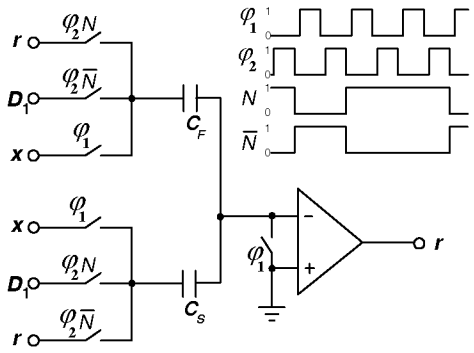

Fig. 3. The 1-bit MDAC in Fig. 2(a) with capacitors C_S and C_F randomly swapped, using a pseudo-random control signal N to digitally measure the capacitor-mismatch error δC using the proposed calibration technique. Note that the values N=0,1 depicted in the figure correspond to the values N=-1,1 used in the text.

D_k is connected to $C_{S,1}$, while D_1 is connected to $C_{S,k}$. Here, D_1 corresponds to the most-significant digit of the sub-ADC output in the multi-bit pipeline stage (Fig. 1) and, hence, is predominantly +1 or -1. Thus, this ensures that the digit connected to the capacitor under calibration in the multi-bit MDAC (Fig. 2b) is predominantly non-zero. It can be shown (as done for the 1-bit MDAC) that such capacitor swapping of $C_{S,k}$ and C_F permits estimating the capacitor-mismatch error δC_k in the digital domain using the iterative relation

$$\hat{\delta}C_k(n+1) = \hat{\delta}C_k(n) - \varepsilon V_{\hat{R}ND}, \quad k = 1,...,2^m - 1 \tag{11}$$

$$V_{\hat{R}ND} = \hat{R}\ N\ D_1 \tag{12}$$

where n is the iteration index and ε is the update step size. Here, $\hat{\delta}C_k$ is the estimated value of the capacitor-mismatch error δC_k. Defining R as the digital representation of the MDAC residue signal r in (10), then $\hat{R}$ is the corrected value of R, after calibration using the estimated values $\hat{\delta}C_k$ for the capacitor-mismatch errors δC_k (k=1, ... , 2^m-1).

III. Interstage-Gain Calibration Technique

Assuming no capacitor mismatches, the residue (output) signal of a switched-capacitor MDAC (Fig. 2) can be expressed as

$$r = (1+\delta g)\left(2^m x - \sum_{i=1}^{2^m-1} D_i V_{ref}\right) \tag{13}$$

where δg represents the gain error due to opamp nonidealities. Unlike the value of capacitor-mismatch error δC in (2), the value of gain error δg in (13) is not constant, but rather a nonlinear function of the residue (opamp-output) signal r. This gain error can be modeled, using an n^{th}-order Taylor-series expansion, as

$$\delta g = \delta g_0 + \delta g_2 r^2 + \delta g_4 r^4 + ... + \delta g_n r^n \tag{14}$$

Here, a fully-differential MDAC is assumed, resulting in a zero value for the odd-order coefficients in the Taylor-series expansion.

In a switched-capacitor MDAC (as in any feedback circuit), nonlinear opamp distortion is reduced by the amount of feedback ($1+A\beta$), where A is the opamp gain and β is the feeback factor. Hence, the effect of nonlinear gain errors is decreased linearly as the opamp dc gain is increased (as shown in Fig. 6).

To measure and correct for the nonlinear gain error δg in a pipeline stage (Fig. 1), a known dither signal (i.e., a pseudo-random sequence *PN)* is added to the input of its sub-ADC. The dither-signal amplitude can be selected such that it does not limit the available analog-signal swing at the pipeline-stage input [10]. In the following, let Y_{PN} denote the output word of the full pipelined ADC, with a dither signal added to the sub-ADC input in the pipeline stage under calibration. Furthermore, let D and D_{PN} denote, respectively, the sub-ADC output with and without a dither signal added at its input.

A. Zero-Order Gain Calibration

Most previously-reported interstage-gain calibration techniques model the gain error δg as a constant error: $\delta g = \delta g_0$ [10]. Gain errors due to δg_0 are then digitally calibrated. For example, in [10], the correlation $cor[PN, Y_{PN}]$ is utilized to calibrate for δg_0. With only errors due to δg_0 in the Taylor-series expansion in (13) being calibrated, this technique is classified as a zero-order gain calibration technique.

B. Second-Order Gain Calibration

In 2nd-order gain calibration techniques, a 2nd order Taylor-series expansion (n=2 in (14)) is utilized to model the nonlinear gain error δg. Gain errors due to δg_0 and δg_2 are then digitally calibrated. For example, in [9], the correlation $cor[PN,Z]$ and the covariance $cov[PN.Z,Z^2]$, where $Z=Y_{PN}-D$, are utilized to calibrate for δg_0 and δg_2, respectively.

C. Fourth-Order Gain Calibration

When using zero- or 2nd-order gain calibration techniques, opamps with high dc gains (≥55dB) are still required to design a high-resolution pipelined ADC (SNDR ≥ 13 bits), as demonstrated by the simulation results in Section IV.

To relax the requirement on the dc gains of the opamps in the MDACs of high-resolution pipelined ADCs, this paper proposes a 4th-order gain calibration technique to digitally measure and correct for interstage-gain errors due to high-order opamp nonidealities. Specifically, define $Z=Y_{PN}-D$. Then, $cor[PN,Z]$ and $cov[PN.Z,Z^2]$ are utilized to calibrate for, respectively, δg_0 and δg_2, as described in [8]. Next, $cov[PN.Z,Z^4]$ is utilized to extend the 2nd-order gain calibration technique in [9] and calibrate for δg_4, as demonstrated by the simulation results in Section IV.

Although the proposed technique for 4th-order gain calibration requires a larger digital logic and, hence, power dissipation to compute Z^4 (compared to only computing Z^2 in the 2nd-order gain calibration method in [9]), it significantly relaxes the requirements on the dc gains of the opamps in the MDACs of a high-resolution pipelined ADC. Thus, significant savings in analog power dissipation can be achieved, as discussed in Section IV.

IV. Simulation Results

A. Digital Calibration of Capacitor Mismatch

The proposed capacitor-mismatch calibration technique is implemented in a 13-bit pipelined ADC. The pipeline core of this ADC is partitioned into a 2.5-bit first stage, followed by eleven 1.5-bit stages. Behavioral simulations of this ADC are performed in SIMULINK, assuming random capacitor-mismatch errors (δC) of 0.25% (1σ) in each pipeline stage. Only the 1st, 2nd, and 3rd pipeline stages of the ADC are calibrated, as its overall performance is most sensitive to the nonidealities in its front-end stages. The measurement and calibration of the capacitor-mismatch errors in these pipeline stages is performed concurrently in the background during the normal ADC operation, with uncorrelated pseudo-random control signals (N) utilized for each stage calibration. In the iterative relations for estimating the capacitor-mismatch errors in equations (8) and (11), the update step size ε is set to 2^{-22}. A full-scale sine wave signal is applied at the ADC input.

Fig. 4 shows the converter SNDR during the initial convergence of the calibration algorithm, while the ADC is in normal operation. Accordingly, to achieve an SNDR ≥ 12 bits (74 dB), the required number of samples is approximately 30x10^6 samples. Such number of convergence samples compares well with that required to achieve a 12-bit resolution using previously-proposed calibration techniques [3, 4].

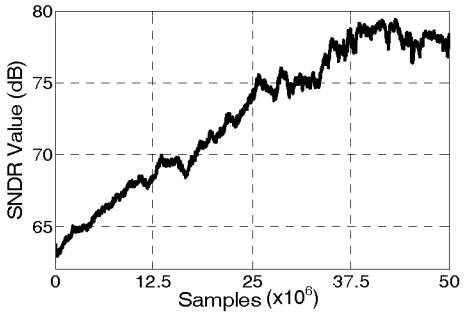

Fig. 4. SNDR value during the normal operation of the pipelined ADC.

TABLE I
SUMMARY OF BEHAVIORAL SIMULATION RESULTS

Swapping / Calibration	SNDR	SFDR
OFF / OFF	62 dB	65 dB
ON / OFF	61.5 dB	79.5 dB
ON / ON	77 dB	95 dB

Fig. 5 shows the output spectrum of the pipelined ADC when performing: (a) no capacitor swapping and no capacitor-mismatch calibration; (b) only capacitor swapping; and (c) both capacitor swapping and capacitor-mismatch calibration. The corresponding SNDR and SFDR of the ADC are summarized in Table I. Accordingly, capacitor swapping by itself only spreads the signal harmonics and, therefore, only improves the SFDR (as in [6]). With both capacitor swapping and capacitor-error calibration, using the proposed capacitor-mismatch calibration technique, a 12.5-bit SNDR and a 95-dB SFDR is achieved for the 13-bit pipelined ADC with $\sigma = 0.25\%$ capacitor-mismatch errors.

B. Interstage-Gain Calibration

To study the effect of interstage-gain errors in high-resolution ADCs, the proposed gain calibration technique is implemented in a 14-bit pipelined ADC. The pipeline core of this ADC is partitioned into a 2.5-bit first stage, followed by twelve 1.5-bit stages. Behavioral simulations of the ADC are performed in SIMULINK. No capacitor-mismatch error is assumed. Furthermore, only the 1st pipeline stage is assumed to have gain errors due to opamp nonidealities in its MDAC. In the behavioral simulations, the following circuit nonidealities of the opamp are modeled [11]:

a) finite and nonlinear dc gain, corresponding to an opamp's input-output transfer curve in the form of a hyperbolic tangent with a maximum dc gain $A_{0,\max}$ and an output saturation voltage $V_{O,\text{sat}}$;

b) dynamic effects (incomplete settling and harmonic distortion), due to finite closed-loop bandwidth BW and slew rate SR;

c) limited output-signal swing, due to a limited $V_{O,\text{sat}}$.

Here, BW=800MHz, SR=1V/ns, and $V_{O,sat}=V_{ref}$=1V are assumed. A 0.95-V 2.5-MHz sinusoidal signal was applied at the ADC input.

Fig. 6 shows the SNDR versus opamp dc gain $A_{0,\max}$, with zero-, 2nd-, and 4th-order gain calibration. Accordingly, to achieve an 80-dB (13-bit) SNDR, opamps with dc gains of 75dB, 62dB, and 53dB are required when using zero-, 2nd-, and 4th-order gain calibration, respectively. Therefore, compared to zero-order [10] and 2nd-order [9] gain-calibration methods, the proposed 4th-order gain-calibration technique relaxes the requirements on the opamp dc gains by 22dB and 9dB, respectively.

Accordingly, high-order gain calibration methods, such as the proposed 4th-order gain-calibration technique, are critical for designing high-resolution high-speed pipelined ADCs in nano-scale CMOS technologies using moderate-gain opamps and, hence, at low power dissipation. In such technologies, opamps with moderate dc gains are readily obtainable using classical folded-cascode or current-mirror designs, however, opamps with high dc gains require either multiple gain stages or output-impedance enhancement, because of the shrinking supply voltages and the poor intrinsic gains of the MOS transistors. Such gain-boosting techniques for the opamps significantly increase the power dissipation and degrade the speed.

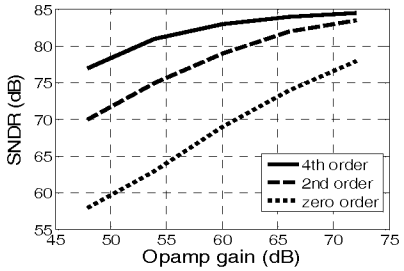

Fig. 6. SNDR vs. opamp dc gain $A_{0,\max}$, with zero-order [10], 2nd-order [9],and 4th-order [this work] interstage-gain calibration.

V. CONCLUSION

Two independent digital background calibration techniques were proposed: 1) a capacitor-mismatch calibration technique and 2) an interstage-gain calibration technique. These techniques are applicable to both 1.5- and multi-bit pipeline stages. Behavioral simulation results confirm their effectiveness in significantly improving the resolution of pipelined ADCs in the presence of large linearity error due to capacitor mismatches and opamp nonidealities.

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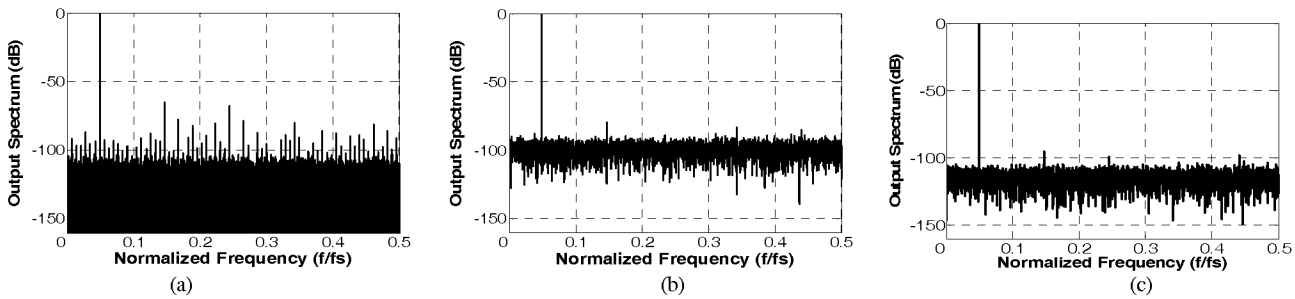

Fig. 5. Output spectrum of the pipelined-ADC when: (a) capacitor swapping is OFF and capacitor calibration is OFF, (b) capacitor swapping is ON and capacitor calibration is OFF, (c) capacitor swapping is ON and calibration is ON.