Analysis of Dynamic Element Matching (DEM) in Pipelined ADCs

Mohammad Taherzadeh-Sani and Anas A. Hamoui
Dept. of Electrical & Computer Engineering, McGill University, Montreal, Canada
{mtaher7 , hamoui}@ece.mcgill.ca

Abstract- **Dynamic element matching (DEM), typically used to enhance the linearity of the digital-to-analog converter (DAC) in a multi-bit ΔΣ modulator, can also be utilized to linearize the sub-DAC in a multi-bit pipeline stage of a pipelined analog-to-digital converter (ADC). In this paper, an analytical approach to estimate the effect of DEM on the spurious-free dynamic range (SFDR) of a pipelined ADC is presented. A closed-form expression for the 3rd-harmonic power and, hence, the SFDR of a pipelined ADC is derived. The proposed analysis shows that performing DEM in the first stage of a pipelined ADC reduces the 3rd-harmonic power in the ADC output spectrum by a factor of (2^m-1), where m is the number of effective bits in the first pipeline stage. Behavioral Monte-Carlo simulations are presented to demonstrate the accuracy of the proposed analysis.**

I. INTRODUCTION

Dynamic linearity is one of the most important specifications of an analog-to-digital converter (ADC), especially in applications requiring high speed and high dynamic range (such as cellular basestation transceivers, multi-standard software radios, medical imaging, ultrasound front-ends, and many other applications). The dynamic linearity of an ADC is commonly formulated as the spurious-free dynamic range (SFDR). The SFDR is defined as the difference, in dB, between the full-scale fundamental tone and the largest spur (harmonic) in the ADC output spectrum.

The pipelined ADC is one of the most popular architectures for high-speed data conversion [1]. The linearity of a pipelined ADC is primarily degraded by the linearity errors in its pipeline stages. Consider a typical pipeline stage with digital redundancy [2], as depicted in Fig. 1. Its linearity is directly limited by that of its digital-to-analog sub-converter (sub-DAC). Achieving high linearity in a multibit DAC requires precise matching of the DAC unit elements. A standard CMOS process typically provides elements with matching no better than 0.1% (10-bit resolution) [3]. Increasing the number of bits in the first stage of a pipelined ADC can relax the requirement on the sub-DAC unit-element matching in its pipeline stages [4,5]. However, there are practical limitations on the maximum number of bits that can be resolved in the first pipeline stage. Therefore, techniques to further enhance the linearity of the multibit sub-DAC in a pipeline stage are needed.

A well-known technique to linearize a multibit DAC is dynamic element matching (DEM) [3]. In DEM, an algorithm dynamically selects different DAC unit elements to represent a given digital input code at different times. This technique, typically utilized to linearize the DAC of a multibit ΔΣ modulator, can also be applied to the sub-DAC of a multibit pipeline stage [6,7].

In a multibit pipeline stage, zero-order DEM can randomize the linearity error due to the sub-DAC nonidealities and, hence, spreads the signal harmonics without correcting for the linearity errors [7,8]. Therefore, the SFDR of the ADC is improved, while its signal-to-noise-and-distortion ratio (SNDR) is not increased because its noise floor is not decreased. Although it has been demonstrated that DEM reduces the power of the signal harmonics due to the sub-DAC nonidealities [6-8], no exact relation has been presented for the harmonic power before and after applying DEM. In this paper, the power of the largest signal harmonic in the output spectrum, and, hence, the SFDR of a pipelined ADC are analyzed and formulated.

This paper is organized as follows: Section II studies the signal harmonics in the output spectrum of a conventional pipelined ADC. Section III analyzes the effect of zero-order DEM (i.e. DAC unit-element randomization) on the signal harmonics in a pipelined ADC and formulates its SFDR. Section IV presents Monte-Carlo behavioral simulation results to demonstrate the accuracy of the proposed closed-form formula.

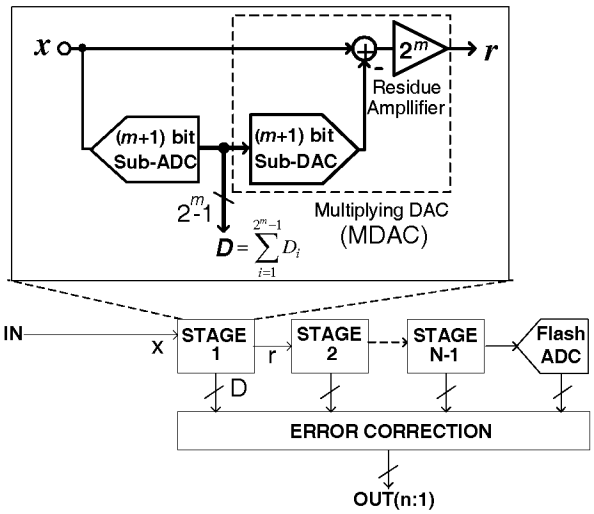


Fig. 1. A generic pipelined ADC structure

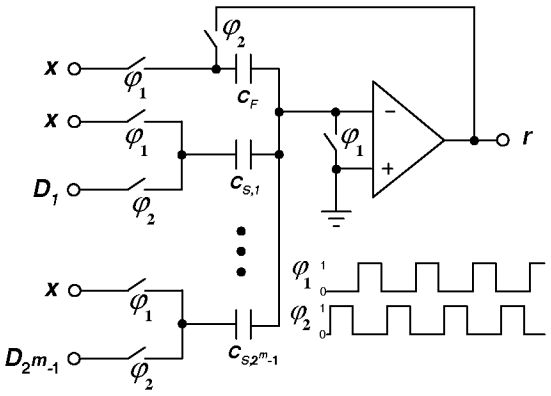


Fig. 2. Capacitor flip-over MDAC for multibit an m-bit pipeline stage (φ_1: the sampling phase and φ_2: the hold phase)

II. Harmonic Distortion in a Conventional Pipelined ADC

Consider the multiplying DAC (MDAC) in Fig. 2, which is widely utilized to realize switched-capacitor (SC) pipeline stages with an m-bit effective resolution. It has 2^m nominally equal capacitors: (2^m-1) sampling/DAC capacitors $C_{S,k}$ (k=1,...,2^m-1) and one feedback capacitor C_F. Its input-output transfer function can be expressed as [9]:

$$r = (1+\delta g)\left(\left(1+\sum_{k=1}^{2^m-1}\frac{C_{S,k}}{C_F}\right)x - \sum_{k=1}^{2^m-1}\frac{D_k C_{S,k}}{C_F}\right) \quad (1)$$

where each digit D_k (k=1,...,2^m-1) is 0 or ± V_{ref}, based on input signal x (i.e., sub-ADC output of the pipeline stage in Fig. 1). Here, δg represents the gain error due to opamp nonidealities. Since the focus of this analysis is on capacitor-mismatch error, δg is assumed to be corrected for by a gain-calibration technique [10] and, hence, a zero gain error (δg=0) is assumed. Furthermore, a unity reference voltage (V_{ref}=1) is assumed for simplicity.

The mismatch error in the kth sampling capacitor (unit element) of the MDAC is defined as:

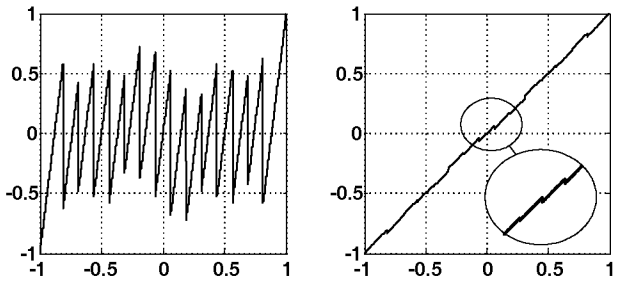
$$\delta C_k = \frac{C_{S,k} - C_F}{C_F} \quad (2)$$

Thus, the expression in (1) can be rewritten as:

$$r = \left(1+\sum_{k=1}^{2^m-1}\frac{\delta C_k}{2^m}\right)2^m x - \sum_{k=1}^{2^m-1}(1+\delta C_k)\cdot D_k \quad (3)$$

Fig. 3 (a) depitcs the transfer function of a nonideal MDAC with 3-bit effective resolution. Figure 3(b) shows the corresponding transfer curve of a pipelined ADC, where this nonideal DAC is utilized in the first pipeline stage (assuming all other stages are ideal).

In general, capacitor-mismatch errors result in a gain error of $\left(1+\sum_{k=1}^{2^m-1}\frac{\delta C_k}{2^m}\right)$ in the transfer function of an MDAC with m-bit effective resolution. When this nonideal MDAC



(a) (b)

Fig. 3. (a) Input-output transfer function of a nonideal MDAC with 3-bit effective resolution; and (b) its effect on the transfer curve of a pipelined ADC, when used in the first pipeline stage.

is utilized in the first pipeline stage of a pipelined ADC, this results in (2^{m+1}-2) breaking points with heights of

$$\Delta_k = \frac{\delta C_k}{2^m} \quad (4)$$

in the input-output transfer curve of the ADC (assuming all other pipeline stages are ideal) [5]. In order to estimate the harmonic component in such an input-output transfer curve, a sinusoidal signal was applied at the input of the ADC and the harmonic components in the output signal were analyzed. It was shown that the even-order harmonic components are zero and the odd-order harmonic components are:

$$a_K = \frac{4}{K\pi}\sum_{k=1}^{2^m-1}\cos\left(K\sin^{-1}\left(\frac{2k-1}{2^{m+1}}\right)\right)\frac{\delta C_k}{2^m} \qquad K>1 \quad (5)$$

The following analysis focuses on the third harmonic, as behavioral simulation results demonstrate that it is the largest one. Since the capacitor-mismatch error is a normally-distributed stochastic variable with a mean value of zero and a standard deviation of $\sigma_{\delta C}$, the third harmonic is also a normal variable with an input-referred variance of:

$$\sigma_{a_3}^2 = \left(\frac{4}{3\pi}\right)^2\sum_{k=1}^{2^m-1}\left(\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^m}\right)\right)\right)^2\frac{\sigma_{\delta C}^2}{2^{2m}} \quad (6)$$

The above expression can be approximated as [5]:

$$\sigma_{a_3}^2 \cong \frac{0.09}{2^{2m}}(2^m-1)\sigma_{\delta C}^2 \quad (7)$$

III. Harmonic Distortion in a Pipelined ADC with DEM-DAC

Dynamic element matching (DEM) is a widely utilized strategy to correct for the DAC nonlinearity due to static mismatch errors between the DAC unit elements. Fig. 4 depicts the MDAC in Fig. 2 (during the hold phase), with a DEM logic block utilized to select the DAC unit elements. Here, for each DAC input code $D_{1...2^m-1}$, the DEM logic block dynamically selects different DAC unit elements (capacitors) to represent a given digital input code at different times [3].

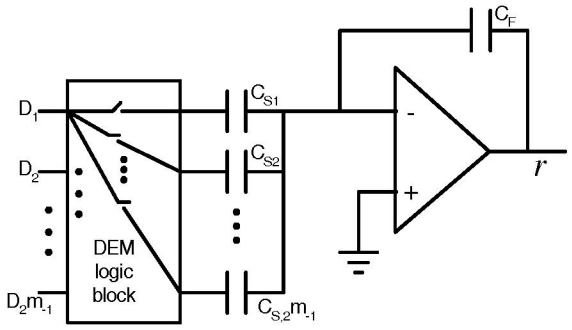


Fig. 4. The m-bit MDAC in Fig. 2 during the hold clock phase, with a DEM logic block

In a switched capacitor DAC, the unit elements are realized using equal capacitors. For an (m+1)-bit DAC, 2^m-1 equal capacitors are utilized (assuming D_k=0 or ±1). Thus, in each clock cycle, there exists $(2^m\text{-}1)!$ different arrangements in which the DEM logic block can connect the capacitors to the input code D. Since a zero-order DEM technique is utilized in this paper, each of these different arrangements for connecting the capacitors can be selected with equal probability. Here, we name the capacitor connected to digit D_k as C_k', which can be any of the $(2^m\text{-}1)$ capacitor C_s depending on the DEM block selection during each clock cycle. Due to static mismatch errors between these capacitors, the input-output transfer curve of the ADC changes slightly depending on which capacitor arrangement is selected by the DEM logic block.

Consider a pipelined ADC, with all pipeline stages but the first stage being ideal. If a sinusoidal signal is applied at the ADC input, the output digital signal can be expressed as

$$X = \left\{B_1(t) f_1(\cos(t)) + \cdots + B_{(2^m-1)!}(t) f_{(2^m-1)!}(\cos(t))\right\} \quad (8)$$

where $f_i(x)$ is the input-output transfer curve of the ADC for each of the DEM-DAC arrangements (i = 1 to $(2^m\text{-}1)!$), and $B_i(t)$ is a binary signal which equals 1 only when the DEM-DAC uses the i-th capacitor arrangement.

Using the Fourier series for each $f_i(x)$ in (8) results in

$$\begin{aligned} X &= \sum_{i=1}^{(2^m-1)!} B_i(t) f_i(\cos(t)) \\ &= \sum_{i=1}^{(2^m-1)!} B_i(t)\left(a_{1,i}\cos(t) + a_{2,i}\cos(2t) + \cdots\right) \end{aligned} \quad (9)$$

where $a_{K,i}$ is the K-th harmonic component of $f_i(\cos(t))$. Rearranging (9) results in

$$\begin{aligned} X &= \sum_{i=1}^{(2^m-1)!}\left(B_i(t)\sum_{K=1}^{\infty} a_{K,i}\cos(Kt)\right) \\ &= \sum_{K=1}^{\infty}\left(\left(\sum_{i=1}^{(2^m-1)!} B_i(t) a_{K,i}\right)\cos(Kt)\right) \end{aligned} \quad (10)$$

Typically (as confirmed by the simulation results), the largest harmonic of each $f_i(x)$ (i.e., $a_{K,i}$) occurs when K=3. It can therefore be assumed that the largest harmonic in X is also the 3rd one. From (10), the 3rd harmonic value of X is

$$a_{X,3} = \left(\sum_{i=1}^{(2^m-1)!} B_i(t) a_{3,i}\right) \quad (11)$$

where $a_{3,i}$ is the 3rd harmonic of the ADC output when the DEM block chooses the ith capacitor arrangement. Since $a_{X,3}$ is not a constant value, an accurate representation of the overall harmonic power can be obtained by taking the overall time-average of $a_{X,3}$. Therefore,

$$a_{X,3} = \frac{1}{T}\int_{-T/2}^{T/2}\left(\sum_{i=1}^{(2^m-1)!} B_i(t) a_{3,i}\right)dt \quad T \to \infty \quad (12)$$

Since the pseudo-random sequence B_i is not periodic, its period is infinity and, thus, the limits of the above integral are assumed to be infinity. Rearranging (12) results in

$$a_{X,3} = \sum_{i=1}^{(2^m-1)!} a_{3,i}\left(\frac{1}{T}\int_{-T/2}^{T/2} B_i(t)dt\right) \quad T \to \infty \quad (13)$$

The value inside the parentheses is the average of $B_i(t)$, which is also its probability of being equal to 1. Since we have a total of $(2^m\text{-}1)!$ different capacitor arrangements, this probability is equal to $1/(2^m\text{-}1)!$ (assuming equal probability for each $B_i(t)$ to be equal to 1). Therefore, expression (13) can be simplified as

$$a_{X,3} = \frac{1}{(2^m-1)!}\sum_{i=1}^{(2^m-1)!} a_{3,i} \quad (14)$$

Substituting (5) into (13) results in

$$a_{X,3} = \frac{1}{(2^m-1)!}\sum_{i=1}^{(2^m-1)!}\frac{4}{3\pi}\sum_{k=1}^{2^m-1}\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^m}\right)\right)\frac{\delta C'_{k,i}}{2^m} \quad (15)$$

where $\delta C'_{k,i}$ is the mismatch between $C'_{k,i}$ and C_F. $C'_{k,i}$ is the sampling capacitor connected to D_k when the DEM DAC uses its i-th capacitor arrangement mode. Rearranging (15) results in:

$$a_{X,3} = \frac{4}{3\pi(2^m-1)!}\sum_{k=1}^{2^m-1}\left(\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^m}\right)\right)\sum_{i=1}^{(2^m-1)!}\frac{\delta C'_{k,i}}{2^m}\right) \quad (16)$$

Therefore, the 3rd-harmonic variance is obtained from

$$\sigma^2_{a_{X,3}} = \left(\frac{4}{3\pi(2^m-1)!}\right)^2\sum_{k=1}^{2^m-1}\left(\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^m}\right)\right)^2\frac{1}{2^{2m}}\sigma^2\left(\sum_{i=1}^{(2^m-1)!}\delta C'_{k,i}\right)\right) \quad (17)$$

When i changes from 1 to $(2^m\text{-}1)!$, the capacitor connected to D_k, $C'_{k,i}$ can be any of the C_S capacitors. Therefore, $\delta C'_{k,i}$ can have only $(2^m\text{-}1)$ different values, which are δC_j (j=1, 2,...,$(2^m\text{-}1)$) defined in (2). Therefore, substituting $\delta C'_{k,i}$ with δC_j in the final term in (17), results in

$$\sum_{i=1}^{(2^m-1)!}\delta C'_{k,i}=\frac{(2^m-1)!}{2^m-1}\sum_{j=1}^{2^m-1}\delta C_j \qquad (18)$$

Therefore,

$$\sigma^2\left(\sum_{i=1}^{(2^m-1)!}\delta C'_{k,i}\right)=\left(\frac{(2^m-1)!}{2^m-1}\right)^2\sum_{j=1}^{2^m-1}\sigma^2_{\delta C_i} \qquad (19)$$

Since all of the capacitors are nominally equal, all $\sigma^2_{\delta C_i}$ are also equal ($=\sigma^2_{\delta C}$). Thus, using (19) in (17) results in

$$\sigma^2_{a_{X,3}}=\frac{1}{(2^m-1)}\left(\frac{4}{3\pi}\right)^2\sum_{k=1}^{2^m-1}\left(\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^m}\right)\right)^2\frac{\sigma^2_{\delta C}}{2^{2m}}\right) \qquad (20)$$

Referring back to the simplification applied to equation (6), equation (20) can be similarly simplified to

$$\sigma^2_{a_3}=\frac{0.09}{2^{2m}}\sigma^2_{\delta C} \qquad (21)$$

Comparing equations (21) and (7) shows that the variance value of the 3rd harmonic is divided by a factor of (2^m-1) when DEM-DAC is employed.

Accordingly, the one-sigma SFDR is obtained from

$$\mathrm{SFDR}=20\log(1/\sigma_{a_3}) \qquad (22)$$

Therefore, since the 3rd harmonic variance is divided by a factor of (2^m-1), the one-sigma SFDR of the pipelined ADC output is improved by $10\cdot\log(2^m\text{-}1)$ dB.

IV. Simulation Results

In order to estimate the value of SFDR, when the statistical behavior of capacitor mismatch is known, a Monte-Carlo simulation, assuming a normal distribution for δC, is performed and the average power of the largest spurious signal is used to extract the value of SFDR.

The proposed equation is tested in a 14-bit pipelined ADC. The pipeline core of this ADC is partitioned into a 2.5-bit first stage, followed by twelve 1.5-bit stages. In the behavioral simulations, the input-output transfer function of the MDAC in each pipeline stage is modeled as in equation (3). Only the 1st pipeline stage is assumed to have capacitor-mismatch errors. Behavioral simulations of the ADC are performed in SIMULINK. Fig. 5 shows the value of the SFDR for different values of $\sigma_{\delta C}$, with DEM (equations (21) and (22)) and without DEM (equations (7) and (22)) applied to the first stage. Also shown are the Monte-Carlo simulation results for different values of $\sigma_{\delta C}$. The figure demonstrates a very good agreement between the proposed equations and the behavioral Monte-Carlo simulations confirming the accuracy of the proposed equations.

V. Conclusion

In this paper, an analytical approach is proposed to investigate the effect of Dynamic element matching (DEM) in pipelined ADC. The analysis shows that performing DEM in the first pipeline stage with m-effective-bit resolution improves the SFDR of the total ADC by $10\cdot\log(2^m\text{-}1)$ dB. Simulation results are presented to confirm the accuracy of the proposed closed form formulas.

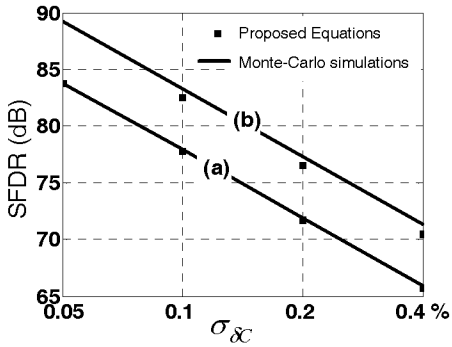


Fig. 5. SFDR vs. $\sigma_{\delta C}$ for a pipelined ADC: (a) without DEM; and (b) with DEM applied to the MDAC in its first pipeline stage

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