Delta-Sigma Modulators for Power-Efficient A/D Conversion in High-Speed Wireless Communications

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Abstract --- This paper describes how the signal path within a ΔΣ modulator can be designed, independent of its noise-shaping characteristics, in order to significantly reduce the harmonic distortion due to opamp nonidealities and to lower the power dissipation. This paper then presents architectural approaches for designing high-resolution ΔΣ modulators at low oversampling ratios (OSRs) and low supply voltages. Thus, analog-to-digital converters (ADCs) can be designed in low-voltage nano-scale digital CMOS technologies to achieve high-speed and high-resolution A/D conversion, with high power efficiency (energy dissipation less than 1pJ per conversion step). Such ΔΣ ADCs are attractive for emerging broadband communication applications.

I. Introduction

The proliferation of broadband digital-communication applications is stimulating research towards the development of analog-to-digital converters (ADCs) with higher speeds and higher resolutions [1]. Example applications include high-speed wireless systems, such as 3G and 4G mobile terminals [2]. These high-speed high-resolution ADCs must be implemented in a standard digital CMOS process to achieve high system integration and low fabrication cost, while harnessing the advanced digital-signal-processing (DSP) capabilities of scaled CMOS processes. However, in nano-scale CMOS technologies, the low supply voltages and the shrinking devices (with poor analog-processing capabilities) complicate the low-power design of high-resolution analog circuits [1].

Oversampling ΔΣ ADCs offer a trade-off in data-converter design: they can achieve high-resolution A/D conversion using low-accuracy analog components, but require higher sampling rates and more complex digital circuits than Nyquist-rate ADCs [3]. Further, oversampling eliminates the need for a precision sample-and-hold circuit and relaxes the requirements on the anti-aliasing filter at the ADC input. Thus, when designing in a standard digital CMOS process, a ΔΣ ADC is particularly attractive for achieving high-resolution A/D conversion in low-to-medium speed applications. Moreover, a ΔΣ ADC is uniquely suited for digital channel-selection in wireless receivers, as both adjacent-channel interferers and out-of-band quantization noise can be suppressed using the same digital decimation filter at the ΔΣ modulator output [4].

However, extending a ΔΣ ADC to high-speed applications requires lowering its oversampling ratio (OSR), such that its ΔΣ modulator is realizable within the technology limitations of CMOS processes and meets a moderate power budget [1]. Unfortunately, this limits the efficiency of the ΔΣ ADC in achieving a high-resolution A/D conversion.

The focus of ΔΣ modulator design has traditionally been on realizing a noise transfer function (NTF) which can achieve a high signal-to-quantization-noise ratio (SQNR) without destabilizing the ΔΣ modulator. This paper describes how the signal transfer function (STF) of a ΔΣ modulator can be designed, independent of its NTF, for unity gain (i.e., STF = 1) in order to:

a) significantly reduce the harmonic distortion due to opamp non-idealities in the integrators of its loop filter [5];

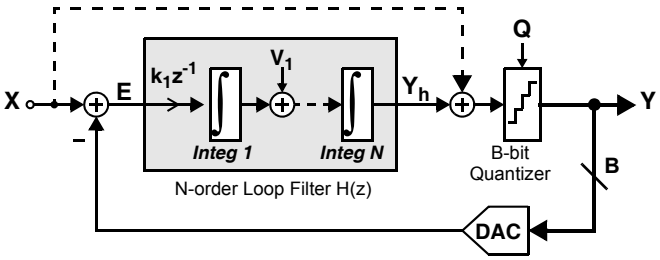

Fig. 1. Linear model of a single-loop ΔΣ modulator (i.e., a ΔΣ modulator with a single DAC feedback). Here, the feedforward signal path (dashed line) can be utilized to achieve an STF = 1, without affecting NTF. Signal V_1 models the circuit noise and distortion error injected at the output of the first integrator stage in the loop filter. Here, $\int \equiv 1/(1-z^{-1})$.

b) help lower the power dissipation, especially for low-OSR ΔΣ ADCs designed in low-voltage digital CMOS technologies.

This paper then describes architectural approaches for designing high-resolution ΔΣ modulators at low OSRs and low supply voltages.

Section II studies the advantages of designing a ΔΣ modulator with a unity-gain STF. Section III then describes how a unity-gain STF can be achieved in ΔΣ modulators with single and distributed DAC feedback. Section IV presents single-stage and cascaded (MASH) architectures for realizing high-resolution ΔΣ modulators at low OSRs and low supply voltages.

II. Advantages of a Unity-Gain STF

The noise and signal transfer functions of the ΔΣ modulator modeled in Fig. 1 are defined, respectively, as:

$$\mathrm{NTF} \equiv Y(z)/Q(z)\big|_{X(z)=0} \quad \text{and} \quad \mathrm{STF} \equiv Y(z)/X(z)\big|_{Q(z)=0} \qquad (1)$$

where $Q(z) \equiv Y(z) - X_q(z)$ is the quantization noise. The error signal at the input of the loop filter $H(z)$ is

$$E(z) \equiv X(z) - Y(z) \equiv [1 - \mathrm{STF}] \cdot X(z) - \mathrm{NTF} \cdot Q(z) \qquad (2)$$

By adding the modulator input signal to the quantizer input signal using the feedforward path (dashed line in Fig. 1), a unity-gain STF

$$\mathrm{STF}(z) = 1 \qquad (3)$$

is achieved [5,7]. This reduces the error signal E (Fig. 1) to

$$E(z) = -\mathrm{NTF}(z)\, Q(z). \qquad (4)$$

Consequently, the loop filter $H(z)$ needs to process only shaped quantization noise, as the analog input signal no longer flows through the loop filter, but rather reaches the quantizer through the feedforward path. Since, ideally, no input signal is processed by the loop filter, no harmonic distortion is generated. Accordingly, the sensitivity of the ΔΣ modulator to opamp non-linearities in the integrators of its loop filter is significantly reduced [5,6].

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A. Low Distortion at Low OSR

The low distortion, achieved by designing the ΔΣ modulator with an STF = 1 (Fig. 1), is particularly notable **at low OSR**, for the following reasons:

1) The sample-to-sample variations in the input signal X and, hence, in the error signal E are substantial at low OSRs. This is even more true with FIR NTFs (discussed in Section IV), whose large out-of band gains amplify the out-of-band noise and cause the unfiltered output waveform Y to deviate by many least-significant bits (LSBs) from the desired output waveform after the decimation filter [8].

2) The attenuation of integrator non-idealities by the ΔΣ loop is inadequate in reducing the distortion appearing at the modulator output Y at low OSRs. For example, consider the 1st integrator stage at the input of the loop filter (Fig. 1). Assume that this integrator stage has a gain k_1 and that the distortion error V_1 at its output can be modelled as additive white noise. Such distortion error will appear high-pass filtered by $(1-z^{-1})/k_1$ at the output of the ΔΣ modulator and, hence, attenuated by a factor of approximately $\pi^2/(3\,k_1^2\,OSR^3)$ within the signal band [1]. Thus, for every factor of 2 lowering in OSR, the attenuation of such distortion by the ΔΣ loop drops by about 9 dB.

B. Low Power

By designing the ΔΣ modulator (Fig. 1) with an STF = 1 and, hence, requiring the opamps in the integrators of loop filter $H(z)$ to process only shaped quantization noise, significant savings in power dissipation can be achieved for the following reasons:

1) Opamp Swing Reduction: With STF = 1, the loop-filter output reduces to $Y_h(z) = -H(z)\,NTF(z)\,Q(z)$ and, hence, becomes independent of the modulator input signal $X(z)$. Thus, the available signal swing at the opamp outputs is no longer shared between the modulator input signal and the shaped quantization noise. As a result, the maximum input-signal amplitude $\|x\|_\infty = max|x(n)|$ is no longer limited by the available swing for $Y_h(z)$. Hence, $\|x\|_\infty$ can be increased with respect to the output saturation voltage $V_{O,sat}$ of the opamp in the last integrator of the loop filter. In fact, the ΔΣ modulator can now tolerate an $\|x\|_\infty = V_{O,sat}$. By contrast, ΔΣ modulators whose signal path goes through $H(z)$ are typically designed for an $\|x\|_\infty$ between 0.5 and 0.8 $V_{O,sat}$ to avoid saturating the opamps [9]. Typically, a switched-capacitor (SC) ΔΣ modulator is designed such that the kT/C noise of the input sampling switches in its 1st integrator stage is the dominant noise source. Therefore, maximizing $\|x\|_\infty$ allows minimizing the input sampling capacitor needed to lower the kT/C noise below the desired noise floor for the ΔΣ modulator. This minimizes the power dissipation needed to achieve a given dynamic range [1]. Such power savings are particularly significant in low-voltage low-OSR ADCs, as the inband signal-to-thermal-noise ratio (due to kT/C noise) is inversely proportional to $\|x\|_\infty^2$ and OSR.

2) Opamp DC Gain: With STF = 1, the linearity requirements on the opamps are relaxed. Hence, by tolerating some gain and phase errors (due to finite opamp gains) in the integrator transfer functions, opamps with only moderate gains can be utilized to realize the integrators [11]. While opamps with moderate dc gains (150 to 300 V/V) are easily obtainable using classical folded-cascode or current-mirror designs, high-gain opamps require either multiple gain stages or output-impedance enhancement due to the low supply voltages and the poor intrinsic gains of the MOS transistors in scaled CMOS technologies. Such gain-boosting techniques significantly increase the power dissipation and degrade the speed [12].

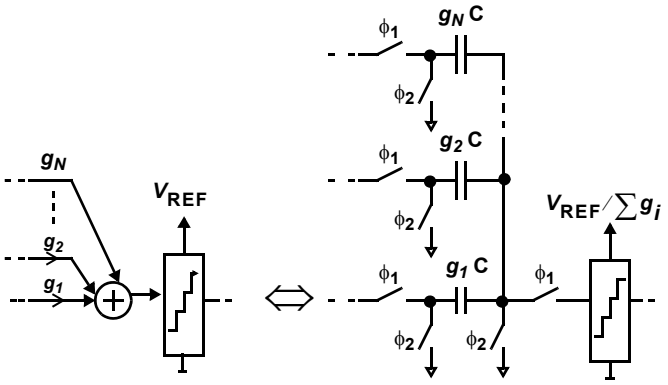


Fig. 2. Passive SC implementation of the summation at the input of the quantizer in a feedforward ΔΣ modulator (a 2-phase non-overlapping clock is assumed). The quantizer's reference voltage V_{REF} is scaled down by a factor of $\sum g_i$ in order to preserve the desired performance for the ΔΣ modulator.
Here, C is an arbitrary unit-size capacitor.

3) Opamp Slew Rate: In a single-stage ΔΣ modulator, the number of delays in the signal path is typically equal to the noise-shaping order N of the loop filter. By designing the ΔΣ modulator with an STF = 1, the signal-path delay is reduced to zero. Decreasing the number of delays in the signal path decreases the sample-to-sample variations in the error signal E at the loop-filter input. As a result, for a targeted settling performance in the SC integrators of the loop filter (especially in the 1st integrator stage, which has the largest impact on the overall modulator performance), the required slew-rate and, hence, power dissipation in the opamps are relaxed [13]. Thus, high-order single-stage ΔΣ modulators can be realized (as described in Section IV) without increasing the requirements on the slew rate and, hence, power dissipation in the opamps of the SC integrators.

In summary, designing a ΔΣ modulator with its loop filter processing only shaped quantization noise (i.e., with an STF = 1 and no input signal X appearing at the outputs of its loop-filter integrators) significantly reduces the modulator sensitivity to SC integrator nonidealities and, hence, helps minimizing the power dissipation[1].

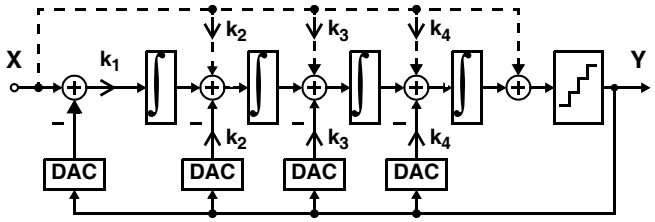
III. Design of Unity-Gain STF

A. Single-Feedback ΔΣ Modulator

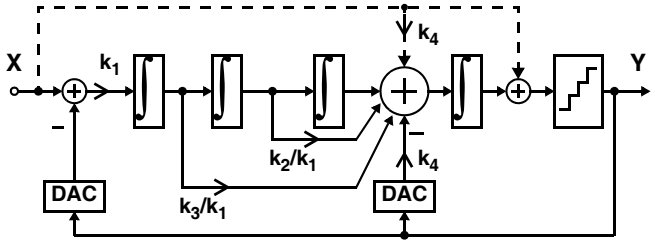
In a ΔΣ modulator with a single DAC-feedback (i.e., a single-loop ΔΣ modulator), an STF = 1 can be achieved without affecting the NTF by adding the modulator input signal to the quantizer input signal, as shown by the feedforward path (the dashed line) in Fig. 1 [14, 7, 5].

In an SC ΔΣ modulator, the summation at the quantizer input can be implemented using the SC network in Fig. 2. If such a passive implementation is used to realize the summation at quantizer input in Fig. 1, the quantizer reference voltage V_{ref} must be scaled down by a factor of 2 from its nominal value. This also scales down (by the same factor) the quantizer step size and, hence, the minimum acceptable accuracy (maximum offset) for the comparators in the quantizer. Accordingly, comparators with a higher resolution will be required.

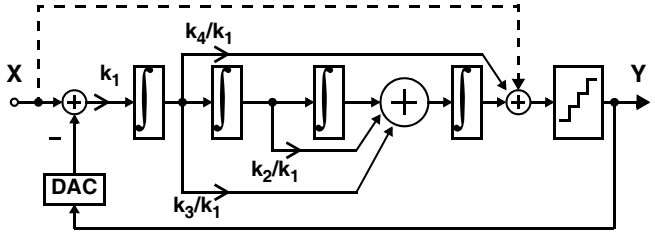
1. Note that, this paper assumes that the loop filter of the ΔΣ modulator processes only shaped quantization noise, when STF = 1. This is the case for all ΔΣ modulators presented in this paper. However, in general, STF = 1 by itself does not guarantee opamp swing reduction, as the loop filter may still process input signal X and the outputs of the loop-filter integrators my contain signal X [6].



(a)



(b)



(c)

Fig. 3. (a): A 4th-order single-stage ΔΣ modulator with a distributed DAC feedback. The dashed feedforward paths can be utilized to achieve an STF = 1, without affecting the NTF [14].
(b) & (c): The feedback paths of the ΔΣ modulator in (a) are replaced with feedforward paths, without affecting the NTF. The dashed feedforward paths are then used to achieve an STF = 1, resulting in modulator topologies that are equivalent to (a), but with reduced input-loading [14].

B. Distributed-Feedback ΔΣ Modulator

In a ΔΣ modulator with distributed DAC-feedback (i.e., a multi-loop ΔΣ modulator), an STF = 1 can be achieved without affecting the NTF by adding the modulator input signal X to the outputs of the loop-filter integrators, as proposed in [14] and shown by the weighted feedforward paths (dashed lines) in Fig. 3(a). This cancels the spectral components of X at these nodes and, consequently, the loop-filter integrators will only have to process shaped quantization noise. A 3rd-order implementation of the ΔΣ modulator architecture in Fig. 3(a) achieved a figure-of-merit of 0.67 pJ/step [15].

However, the above technique significantly increases the loading at the modulator input. An alternative approach (Fig. 3(b)) is to first replace the distributed feedback paths, except for the first and last paths, with feedforward paths without affecting the NTF. Then, to achieve an STF = 1, the input signal X needs to be added only to the outputs of the last two integrators, as shown by the dashed lines in Fig. 3(b) [14].

A further reduction in the input loading can be achieved by mapping the distributed-DAC-feedback ΔΣ modulator into a single-DAC-feedback structure without affecting the NTF (Fig. 3(c)). Then, to achieve an STF = 1, the input signal X needs to be added to the output of only the last integrator, as shown by the dashed lines in Fig. 3(c) [14]. However, in this case, a passive SC implementation of the summation at the quantizer input may not be practical (due to the associated constraints on the comparator offsets, as described above) and an active weighted-summation amplifier may be required.

IV. High-Resolution ΔΣ Modulators at Low-OSR and Low-Voltage

The simplest NTF, which can achieve a high SQNR at a low OSR, is a high-pass finite-impulse response (FIR) function with N zeros at dc. For an N-order ΔΣ modulator (Fig. 1), the attainable SQNR can be further increased by shifting two NTF complex-conjugate zeros from dc to a frequency f_0 (within the signal band $[0, f_{BW}]$) in a manner that minimizes the inband quantization-noise power.
For $N \geq 2$, this corresponds to

$$NTF = (1 - z^{-1})^{N-2}(1 - \delta z^{-1} + z^{-2}) \qquad (5)$$

where $\delta \equiv 2\cos(2\pi f_0/f_s)$ and f_s is the sampling frequency [14]. This results in the high-pass NTF characteristic having a notch at frequency f_0.

Assuming additive white quantization noise and a brick-wall decimation filter, the optimal placement of the complex-conjugate NTF zeros is at approximately $f_0 = \sqrt{(2L-3)/(2L-1)}\, f_{BW}$ and results in

$$SQNR = \frac{3}{2}\,\pi\, A_{OL}^2\,(2^B - 1)^2 \left(\frac{\mathrm{OSR}}{\pi}\right)^{2N+1} (2N+1)\,(L-0.5)^2 \qquad (6)$$

where $A_{OL} = \|x\|_\infty / V_{ref}$ is the quantizer overload ratio, $\|x\|_\infty$ is the maximum amplitude of the input sine-wave signal X, and V_{ref} is the quantizer reference voltage (full-scale range / 2) [1]. This corresponds to a factor of $(N-0.5)^2$ improvement in SQNR relative to when all NTF zeros are at dc [1]. (For example, with $N = 4$, $f_0 = 0.845\, f_{BW}$ results in an 11-dB $SQNR$ improvement, relative to $f_0 = 0$). Therefore, compared to spreading all the NTF zeros across the signal band as in [16], shifting only one pair of complex-conjugate zeros closer to f_{BW} still results (independent of the OSR) in a substantial gain in SQNR, while requiring a much simpler circuit implementation (as described below). Hence, this technique is particularly attractive at low OSRs [14]. In practice, the position f_0 of the notch in the NTF high-pass characteristic should be optimized taking into account the non-ideal frequency response of the decimation filter. In general, simulations show that the SQNR sensitivity to the optimal f_0 is inherently low [17].

An FIR NTF results in an STF with a gain of approximately[1] unity within the signal band, but with a high-pass overall characteristic. Thus, in addition to the advantages discussed in Section II, a flat unity-gain STF (i.e., $|\mathrm{STF}| = 1$ over all frequencies) is further desirable in the case of an FIR NTF, since: **a)** it relaxes the requirements on the anti-aliasing filter preceding the ΔΣ modulator; and **b)** it enhances the stability of the ΔΣ modulator by reducing the out-of-band spectral components in the quantizer's input signal (due to electronic noise, and when the modulator is driven by large transient signals with significant out-of-band energy), which may otherwise overload the quantizer.

1. For $\mathrm{OSR} \geq 8$, $-0.3\,\mathrm{dB} \leq |STF| \leq 0.3\,\mathrm{dB}$ within the signal band.

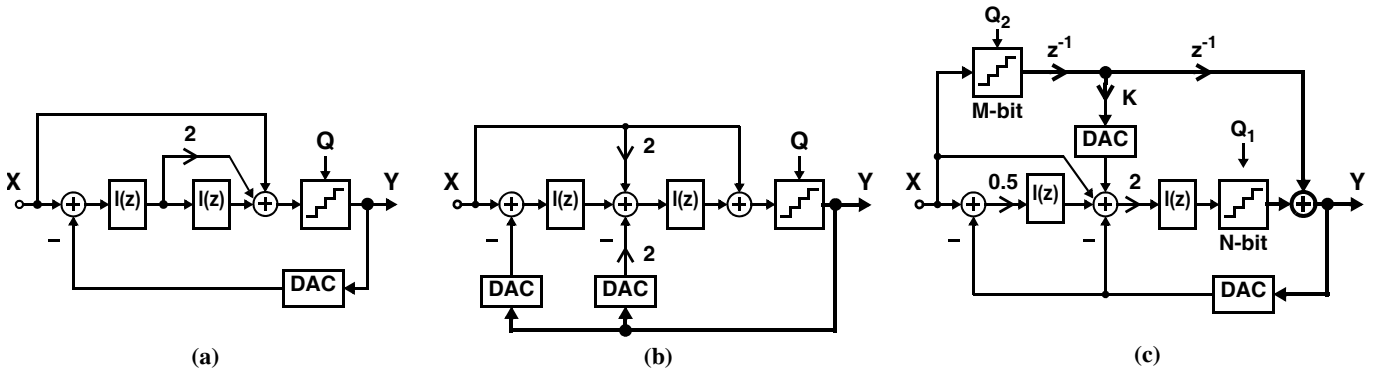


Fig. 4: 2nd-order ΔΣ modulators with an FIR NTF and unity-gain STF. (Here, $I(z) \equiv 1/(1-z^{-1})$)
(a) single DAC-feedback achitecture with analog forward paths [5];
(b) distributed DAC-feedback architecture with analog forward paths [14];
(c) distributed DAC-feedback architecture with digital forward paths ($K = -(1-z^{-1})/2$) [18].

A. 2nd-Order Single-Stage ΔΣ Modulators

Figure 4 shows three 2nd-order ΔΣ modulator architectures, each with an STF=1 and an FIR NTF having all its zeros at dc. In Fig. 4(a) and (b), the feedforward path is implemented in the analog domain. A low-power solution for implementing the analog summation at the quantizer input in Fig. 4 (a) and (b) is using the SC capacitor network in Fig. 2. However, such an implementation is only effective when the number of quantization bits and, hence, the quantizer input capacitance is small. An improved solution, which is effective when the number of quantization bits is large, is to move the feedforward path to the digital domain, as shown in Fig. 4(c) [18]. This requires a quantized version of the input signal of the ΔΣ modulator, which is obtained using a 2nd coarse quantizer. The additional block K and the unit delay in Fig. (c) are used to eliminate the effect of the quantization noise of the 2nd quantizer at the output of the ΔΣ modulator. Simulation results presented in [18] show that a 5% mismatch in the 2nd-integrator coefficient is still acceptable without distortion. An implementation of this architecture achieved a figure-of-merit of 0.48 pJ/step [19].

B. MASH Architectures

Stable high-order ΔΣ modulators can be designed by cascading 1st- or 2nd-order ΔΣ modulator stages in a MASH architecture [9]. MASH architectures require coupling the quantization noise from one modulator stage to the next stage in the cascade. This typically implies subtracting the quantizer output from its input, which requires extra circuitry. An example of a MASH architecture with two cascaded stages is shown in Fig. 5(a). The 2nd-order ΔΣ modulator with a unity-gain STF and a 2nd-order FIR NTF in Fig. 4(a) is particularly suited for MASH architectures, as the quantization error is directly available at the output of the 2nd integrator [20]. Thus, the 1st stage can be directly connected to the 2nd stage when using this modulator to build the stages of a MASH architecture, as depicted in Fig. 5(b). This reduces the sensitivity of the MASH ΔΣ modulator to circuit nonidealities [20]. An implementation of the architecture in Fig. 5(b) achieved a figure-of-merit of 1pJ/step [22].

C. High-Order Multibit Single-Stage ΔΣ Modulators

At low OSRs, the loss in SQNR can be compensated for by increasing the noise-shaping order N of the loop filter and/or the resolution of the B-bit quantizer (Fig. 1). The impact of increasing the order N on the SQNR diminishes significantly as the OSR is reduced. In contrast, the effectiveness of increasing the number of quantization bits B is independent of the OSR, as per equation (6). Other advantages of multibit quantization include: **a)** enhanced modulator stability, enabling the realization of high-order single-stage ΔΣ modulators [14]; and **b)** relaxed slew-rate and settling requirements on the opamps in the loop-filter integrators, enabling further savings in power dissipation [11]. However, the linearity of a multibit ΔΣ modulator is limited by that of its multibit feedback DAC. Fortunately, linearization techniques, such as the Pseudo Data-Weighted-Averaging (Pseudo DWA) technique propose in [14] can be used to correct for the mismatch errors in the DAC elements.

A high-order ΔΣ modulator with a single-stage architecture (rather than a MASH topology) is much less sensitive to the finite dc gains of the opamps. Furthermore, a single DAC-feedback (rather than a distributed DAC-feedback) within a single-stage multibit ΔΣ modulator significantly reduces the complexity of implementing the analog and DAC-linearization circuits, the chip area, and the power dissipation, especially when bootstrapped switches are needed in low-voltage designs [21].

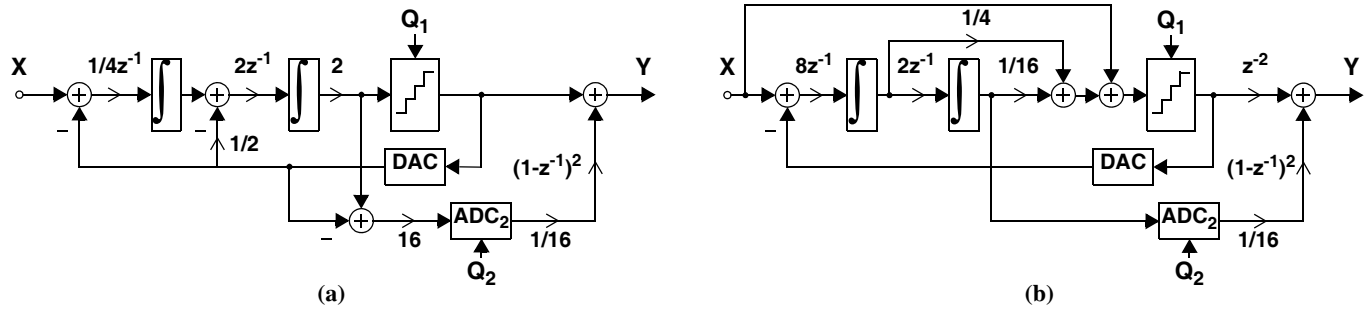
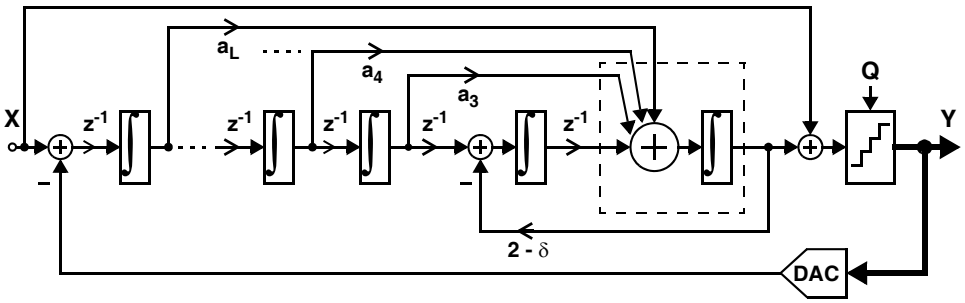


Fig. 5: 2-0 MASH Architecture: a) traditional topology; and b) topology using the modulator stage in Fig. 4(a).



L	a_3	a_4	a_5	a_6
3	δ + 1			
4	$2 + 2z^{-1}$	δ + 2		
5	5	5	δ + 3	
6	4 and $2z^{-1}$	9	11	δ + 4

Fig. 6. High-order multibit ΔΣ modulator with FIR NTF and unity-gain STF [14]. The feedforward coefficients a_k ($k = 3, \ldots, N$) needed to realize the FIR NTF in equation (5) are given in the table. Here $\int \equiv 1/(1-z^{-1})$. Compared to traditional single-stage feedforward architectures, it acheives reduced circuit complexity, reduced sensitivity to coefficient variations, and reduced spread in coefficient ratios .

Accordingly, the single-stage multibit ΔΣ modulator with single-DAC-feedback in Fig. 6 was proposed in [14] to implement the *N*-order FIR NTF in equation (5) and an STF = 1. Compared to a traditional feedforward ΔΣ modulator [24-26], the high-order multibit ΔΣ modulator in Fig. 6 offers the following advantages [14]: **1)** reduced circuit complexity, by not requiring a weighted summation amplifier before the quantizer, as the summation of the signals in the feedforward paths is performed within the last integrator stage of the loop filter; **2)** reduced sensitivity to process variations in the modulator coefficients, owing to the reduced number of feedforward paths (as every feedforward path corresponds to a cancellation in the NTF and STF); and **3)** reduced spread in coefficient ratios.

The block model of the ΔΣ modulator in Fig. 6 can be directly mapped to a SC circuit. Except for the finite-zero loop-gain parameter δ, the modulator coefficients are independent of OSR and f_S. The implementation of the complex-conjugate NTF zeros is achieved by one additional local feedback path around the last two integrators in the loop filter (thereby forming a resonator) and, hence, requires very little analog circuitry. Although integrators with both delaying and non-delaying paths are required to implement an FIR NTF, the high-frequency settling properties of the ΔΣ modulator are enhanced by designing it with no delay-free loops and by interconnecting the loop-filter integrators such that the worst-case settling when δ = 2 corresponds to two opamps settling in series.

An implementation of the architecture in Fig. 6 achieved a figure-of-merit of 0.7 pJ/step [23].

V. Acknowledgment

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