Digitally-Enhanced 2nd-Order ΔΣ Modulator with Unity-Gain Signal Transfer Function

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ABSTRACT

Low distortion and reduced swing can be achieved by designing the ΔΣ modulator with an input feedforward path. Furthermore, the modulator stability can be enhanced and the requirements on the preceding anti-aliasing filter can be relaxed by designing the ΔΣ modulator for a flat unity-gain signal transfer function (STF). Previously-developed ΔΣ modulators with analog feedforward (AFF) achieved a unity-gain STF. However, their performance is limited by the need for an analog adder before the quantizer. Previously-developed ΔΣ modulators with digital feedforward (DFF) eliminated the need for this analog adder. However, their STF was not unity. In this paper, a technique for designing digitally-enhanced ΔΣ modulators with both a DFF path and a unity-gain STF is presented. A 2nd-order DFF ΔΣ modulator with a unity-gain STF is then proposed. Its key features include reduced signal swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, and robustness to ΔΣ modulator coefficient variations. Behavioral simulation results confirm its performance advantages versus previously-developed AFF and DFF ΔΣ modulators.

I. INTRODUCTION

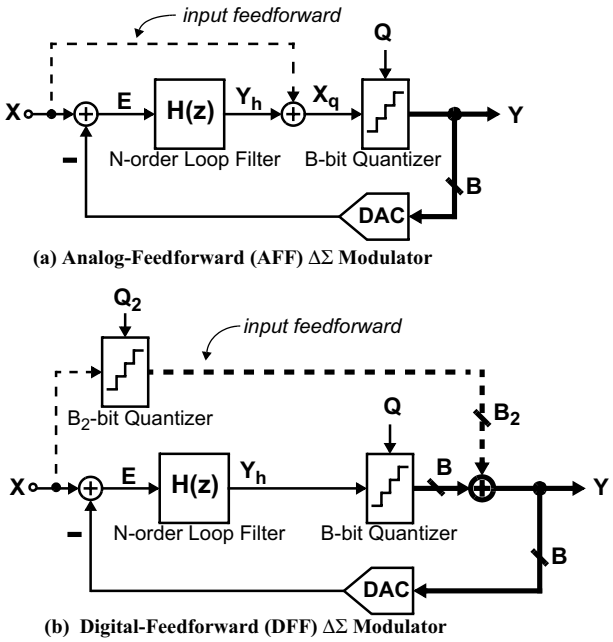
High-speed high-resolution analog-to-digital converters (ADCs) for broadband digital communications must be implemented in standard digital CMOS processes for higher integration of the analog and digital functions and for reduced cost. However, the low supply voltages in nanometer CMOS processes limit the signal swing, thus complicating the design of low-power ADCs.

Oversampling ΔΣ ADCs offer a trade-off in data-converter design: they can achieve a high-resolution A/D conversion using low-accuracy analog components, but require higher sampling rates and more complex digital circuits than Nyquist-rate ADCs. Furthermore, oversampling eliminates the need for a precision sample-and-hold circuit and relaxes the requirements on the anti-aliasing filter at the ADC input [1]. Accordingly, when designing in a standard digital CMOS technology, ΔΣ ADCs are particularly attractive for achieving a high-resolution A/D conversion in low-to-medium speed applications. However, extending a ΔΣ ADC to high-speed applications requires lowering its oversampling ratio (OSR) to realize its ΔΣ modulator within the technology limitations of CMOS processes and to meet a moderate power budget.

The input feedforward path in a ΔΣ modulator is an attractive technique for low-distortion swing-reduction design (Fig. 1) [2,3]. Consider the ΔΣ modulators modeled in Fig. 1. Their signal and noise transfer functions are defined, respectively, as:

$$\text{STF} \equiv Y/X\big|_{Q=0} \quad \text{and} \quad \text{NTF} \equiv Y/Q\big|_{X=0} \tag{1}$$

With an input feedforward path (dashed line in Fig. 1), the input signal of the modulator no longer flows through the loop filter, but rather reaches the modulator output through the feedforward path [2]. Since, ideally, the input signal is not processed by the opamps in the loop-filter integrators, no harmonic distortion is generated and the signal swing is reduced at the integrator outputs [3]. The reduced distortion, achieved by designing the ΔΣ modulator with an input feedforward path, is particularly noticeable at low OSR and



(a) Analog-Feedforward (AFF) ΔΣ Modulator

(b) Digital-Feedforward (DFF) ΔΣ Modulator

Fig. 1. Linear model of a single-stage ΔΣ modulator with an input feedforward path (dashed line) implemented in: a) the analog domain; and b) the digital domain.

low supply voltages [2]. This is because, for a given input-signal swing, lowering the supply voltage increases the nonlinear distortion appearing at the output of the loop filter. Furthermore, at low OSR, the attenuation of the analog-circuit nonidealities by the ΔΣ loop is inadequate in reducing the nonlinear distortion appearing at the output of the ΔΣ modulator. Hence, the input feedforward path helps lower the power dissipation, especially for low-OSR ΔΣ modulators designed in low-voltage nanometer CMOS technologies [2].

The input feedforward path can be implemented using either the analog feedforward (AFF) path in Fig. 1a or the digital feedforward (DFF) path in Fig. 1b. Previously-reported ΔΣ modulators with an AFF path had a unity-gain STF (i.e., $|\text{STF}| = 1$) and a 2nd-order [3,4] or high-order [2] NTF. Previously-reported ΔΣ modulators with a DFF path had a 2nd-order NTF, however their STF was not unity [5].

In this paper, the advantages and design challenges of a ΔΣ modulator with a DFF versus AFF path are outlined and the advantages of a unity-gain STF are described (Section II). Next, a general architecture for digitally-enhanced ΔΣ modulators with a unity-gain STF is presented. A 2nd-order DFF ΔΣ modulator with a unity-gain STF is then proposed (Section III). Its key features include reduced signal swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, and robustness to ΔΣ modulator coefficient variations. Behavioral simulation results are presented to confirm the performance advantages of the proposed 2nd-order DFF ΔΣ modulator with $|\text{STF}| = 1$ versus previously-reported AFF and DFF ΔΣ modulators (Section IV).

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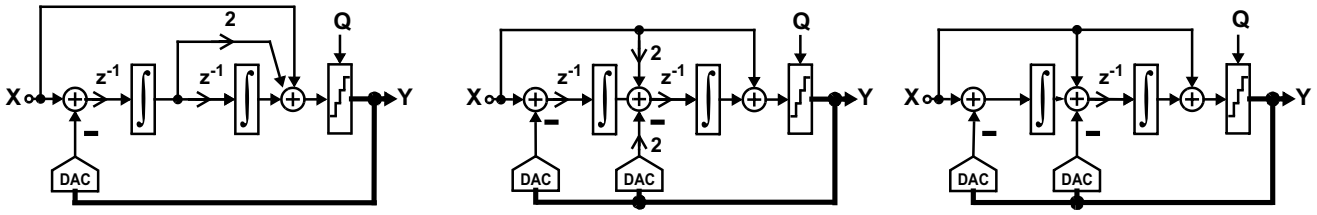

Fig. 2. 2nd-order AFF ΔΣ modulators with NTF = $(1-z^{-1})^2$ and STF = 1 : (a) Single DAC-feedback [3]; (b) and (c) Distributed DAC-feedback [2,4]. Here, $\int \equiv 1/(1-z^{-1})$.

II. AFF vs. DFF ΔΣ Modulators and Unity-Gain STF

A. Analog Implementation

The 2nd-order ΔΣ modulators with AFF path in Fig. 2 have been designed for [3,4]:

$$NTF(z) = (1-z^{-1})^2 \quad \text{and} \quad STF(z) = 1 \tag{2}$$

However, the implementation of an AFF path is complicated by the need for an analog adder to realize the summation at the quantizer input. This analog adder can be implemented using:

a) an active analog summation amplifier [6]. However, since this analog amplifier must process the full-scale analog input signal, the signal swing at the modulator input will be limited by the available signal swing at the output of the analog amplifier. Furthermore, the need for active components (opamps) when using an active amplifier increases the overall power dissipation.

b) a passive switched-capacitor (SC) network [2]. This low-power solution is only effective when the number of quantization bits and, hence, the quantizer input capacitance is small. However, in the case of multibit quantization, a buffer is needed between the SC network and the quantizer for proper operation. Furthermore, to maintain the signal swing at the quantizer input, the quantizer reference voltage must be scaled down from its nominal value by a factor equal to the voltage drop across the passive SC network [2]. This also scales down (by the same factor) the quantizer step size and, hence, the minimum acceptable accuracy (maximum offset) for the comparators in the quantizer. Therefore, comparators with a higher resolution are required.

B. Digital Implementation

To overcome the drawbacks of an analog implementation, the input feedforward path can be implemented in the digital domain (Fig. 1b). The 2nd-order ΔΣ modulator with DFF path in Fig. 3 has been designed for [5]:

$$NTF(z) = (1-z^{-1})^2 \quad \text{and} \quad STF(z) = 1 - NTF(z) \tag{3}$$

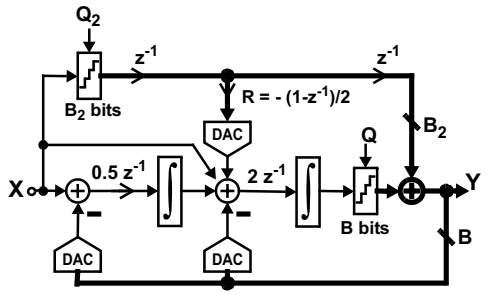

Fig. 3. 2nd-order DFF ΔΣ modulator with NTF = $(1-z^{-1})^2$ and STF = 1 − NTF [5]. Here, $\int \equiv 1/(1-z^{-1})$.

This requires an extra quantizer. However, owing to the reduced signal swing with DFF, the total number of comparators required in the main and the extra quantizers of a DFF modulator is minimally larger than that required in an AFF modulator with equivalent noise-shaping characteristics (as shown in Section IV). Furthermore, although the extra quantizer injects additional quantization noise Q_2 at the modulator output, the feedforward path with gain R in Fig. 3 is utilized to cancel the effect of Q_2 at the output of the DFF ΔΣ modulator.

C. Unity-Gain STF

In a classical ΔΣ modulator (Fig. 1a without the feedforward path) or in the DFF ΔΣ modulator in Fig. 3:

$$STF(z) = 1 - NTF(z). \tag{4}$$

An N^{th}-order finite-impulse-response (FIR) NTF,

$$NTF(z) = (1-z^{-1})^N, \tag{5}$$

results in an STF in equation (4) with a gain $|STF(f)|$ of approximately[1] unity within the signal band, but with a high-pass characteristics (as depicted in Fig. 4). A flat unity-gain STF (i.e., $|STF(f)| = 1$ over all frequencies) is more desirable for the following reasons:

1) it relaxes the requirements on the anti-aliasing filter preceding the ΔΣ modulator.
2) it enhances stability of the ΔΣ modulator by reducing the out-of-band spectral components in the signal at the quantizer input (due to electronic noise and when the modulator is driven by large transient signals with significant out-of-band energy), which may otherwise overload the quantizer.

Accordingly, to harness the advantages of both the DFF path and the unity-gain STF, a DFF ΔΣ modulator with STF=1 is proposed in the following section.

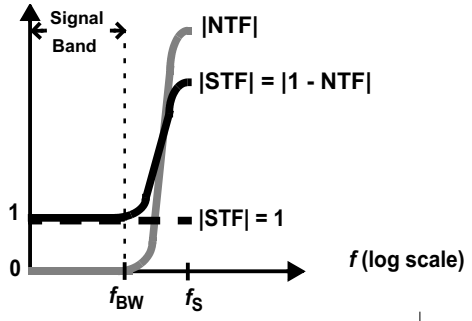

Fig. 4. Sketch of the magnitude responses: $|NTF| = \left|(1-z^{-1})^N\right|$ of an FIR NTF; $|STF| = |1-NTF|$ of the resulting STF; and $|STF| = 1$ of a unity-gain STF.

1. For OSR ≥ 8, −0.3dB ≤ |STF(f)| ≤ 0.3dB within the signal band.

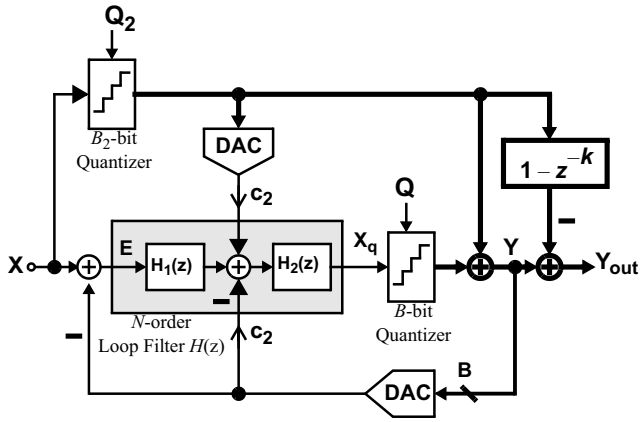

Fig. 5. Proposed architecture for a ΔΣ modulator with DFF and unity-gain STF.

III. PROPOSED DFF ΔΣ MODULATOR WITH |STF|=1

A. General Architecture for a DFF Modulator with |STF|=1

Consider the ΔΣ modulator architecture proposed in Fig. 5. Here, the input feedforward path is implemented in the digital domain. To process the additional quantization noise Q_2 without affecting the STF, the difference between the output of the extra B_2-bit quantizer and the output of the ΔΣ modulator is applied at the output of the loop-filter integrators. The loop filter is then designed such that the modulator output is

$$Y = X + (1 - z^{-1})^N Q + (1 - z^{-K})\, Q_2 \tag{6}$$

where N is the order of the loop filter and K is a design parameter. Next, to cancel the additional quantization noise Q_2 at the modulator output, the output $(X + Q_2)$ of the extra B_2-bit quantizer is multiplied by $(1 - z^{-K})$ and subtracted from the output of the main quantizer in the digital domain. Thus, the overall output of the ΔΣ modulator is then given by

$$Y_{\text{out}} = STF \cdot X + NTF \cdot Q \tag{7}$$

where $STF = z^{-K}$ and $NTF = (1 - z^{-1})^N$

Accordingly, the DFF ΔΣ modulator can be designed for an FIR NTF and a unity-gain STF ($|\text{STF}| = 1$). Furthermore, the loop filter processes only shaped quantization noise

$$E = -NTF \cdot Q - (1 - z^{-K}) Q_2 \tag{8}$$

and the quantizer input (loop-filter output) includes only shaped quantization noise

$$X_q = (NTF - 1) \cdot Q - z^{-K} Q_2 \tag{9}$$

Thus, the voltage swing is reduced at the internal nodes of the loop-filter integrators and at the input of the main B-bit quantizer.

Observe that analog-circuit nonidealities can cause incomplete cancellation of the term $(1 - z^{-K})\, Q_2$ at the modulator output. Therefore, designing for $K = 1$ ensures that any leakage of the additional quantization noise Q_2 to the modulator output (due to incomplete cancellation) is 1st-order shaped. This minimizes the sensitivity of the ΔΣ modulator to the finite dc gains of the opamps and to the variations in the loop-filter coefficients, compared to any other choice of K (as demonstrated by the behavioral simulation results in Section IV).

K	a_1	a_2	c_2
1	1	z^{-1}	z^{-1}
2	z^{-1}	z^{-1}	$2z^{-1}$

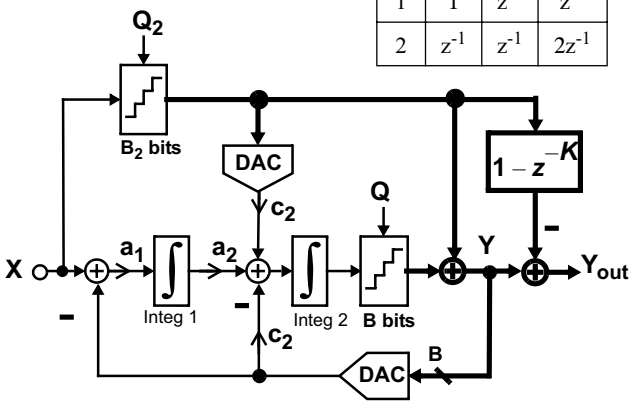

Fig. 6. Proposed 2nd-order DFF ΔΣ modulator with $NTF = (1 - z^{-1})^2$ and $STF = z^{-K}$, for $K = 1$ or $K = 2$. The corresponding feedforward coefficients are given in the table.

B. Proposed 2nd-order DFF ΔΣ Modulator with |STF| = 1

Based on the proposed design concept in Fig. 5, the 2nd-order DFF ΔΣ modulator in Fig. 6 is proposed to realize

$$NTF = (1 - z^{-1})^2 \quad \text{and} \quad STF = z^{-K} \tag{10}$$

with $K = 1$ or $K = 2$.

IV. BEHAVIORAL SIMULATION RESULTS

A. Behavioral Simulation Conditions and Models

The proposed DFF ΔΣ modulator (Fig. 6) and the previously-reported AFF (Fig. 2b) and DFF (Fig. 3) ΔΣ modulators were simulated in SIMULINK for the following design specifications:

- 16-level mid-tread quantizers ($B = B_2 = 4$ bits) and OSR = 32.
- The quantizer reference voltage is normalized to $V_{\text{REF}} = 1$ V.
- The amplitude of the sinusoidal input signal is $V_{\text{in}} = 0.5$ V (-6 dBFS).
- The input-signal frequency is set to $f_{\text{in}} = f_S/(8 \cdot \text{OSR})$, so that the first 4 input-signal harmonics to fall within the signal band.

The SIMULINK behavioral simulations accounted for the following loop-filter nonidealities:

1) Opamp Nonidealities: The integrators in the ΔΣ loop filter are modeled as described in [7] to account for the finite dc gains, the nonlinear dc-gain variations, and the output saturation voltages of the opamps in practical switched-capacitor (SC) integrators. These opamps are assumed to have a **maximum dc gain** $A_{\mathbf{0max}} = 150$V/V (43 dB) and an output saturation voltage $V_{\text{Osat}} = 1$ V. This is to account for the low dc gains of the opamps in nanometer CMOS technologies. In these scaled technologies, high-gain opamps require either multiple gain stages or output-impedance enhancement, due to the low supply voltages and the poor intrinsic gains of the MOS transistors. Such gain-boosting techniques for the opamps significantly increase the power dissipation and degrade the speed.

2) Modulator Coefficients: To account for variations in modulator coefficients, the signal-to-noise-plus-distortion ratio (SNDR) values reported correspond to the minimum SNDR values found over 50 simulations in which each modulator coefficient is assumed to have a **uniformly-distributed random error** in the range $\pm\, e_{\mathbf{coeff}} = 1\%$.

B. Behavioral Simulation Results

Table I summarizes the behavioral simulation results. Accordingly, the proposed DFF ΔΣ modulator (Fig. 6 with K=1) achieves comparable SNDR and output-swing reduction, as the previously-reported DFF ΔΣ modulator (Fig. 3). Observe that the signal swing at the quantizer input is much more reduced in the proposed DFF ΔΣ modulator, compared to the previously-reported AFF ΔΣ modulator (Fig. 2b). This is because, in the AFF modulator, the full-swing input signal X appears at the quantizer input. Whereas, in the proposed DFF modulator, no input-signal component appears at the input of the main quantizer and only shaped quantization noise is processed by the main quantizer (Section III). Owing to this swing reduction (shown in Table I), the number of comparators needed in the main quantizer of the proposed DFF modulator can be reduced from 16 to $16 \times 0.22 \rightarrow 4$. Accordingly, the total number of comparators required in the main and the extra quantizers of the proposed DFF modulator is only increased by 4, relative to that required in the AFF modulator.

Figure 7 shows the swing distribution at the output of each integrator in the ΔΣ loop filter. Accordingly, the swing reduction in the proposed DFF ΔΣ modulator is comparable to that in the AFF ΔΣ modulator.

Figure 8a shows the SNDR versus the maximum dc gain $A_{0\max}$ of the opamps in the SC integrators of the ΔΣ loop filter, assuming an error of e_{coeff} = 1% in the modulator coefficients. Accordingly, the sensitivity of the proposed DFF modulator (with K = 1) to nonlinear variations in opamp dc gains is comparable to that of the previously-reported AFF and DFF ΔΣ modulators. Furthermore, the proposed DFF ΔΣ modulator can achieve a high resolution and linearity (SNDR > 12 bits at V_{in} = –6 dBFS), using opamps with only moderate dc gains (less than 200 V/V). This confirms the reduced sensitivity of the proposed DFF ΔΣ modulator to opamp dc gains.

Figure 8b shows the SNDR versus error e_{coeff} in the modulator coefficients, assuming a maximum dc gain $A_{0\max}$ =150V/V (43dB) for the opamps. Accordingly, the proposed DFF ΔΣ modulator with K = 1 can tolerate a 2% variation in its loop-filter coefficients with only 1.6-dB drop in SNDR. However, the SNDR of the previously-reported AFF and DFF ΔΣ modulators drops by 2.9 dB and 0.9 dB, respectively. This confirms the robustness of the proposed DFF ΔΣ modulator to variations in the modulator coefficients.

TABLE I COMPARISON BETWEEN AFF AND DFF ΔΣ MODULATORS

Configuration	AFF modulator [2,4] (Fig. 2b)	DFF modulator [5] (Fig. 3)	Proposed DFF modulator (Fig. 6)	
	B = 4 bits	$B = B_2$ = 4 bits	$B = B_2$ = 4 bits	
			K = 2	K = 1
SNDR at V_{in} = - 6dBFS with $A_{0\max}$ = 150V/V ± e_{coeff} = 1%	77.9	74.7	71.3	72.4
1st-integrator Output Swing (absolute maximum)	0.11	0.06	0.21	0.17
2nd-integrator Output Swing (absolute maximum)	0.17	0.21	0.21	0.22
Quantizer Input Swing (absolute maximum)	0.66	0.21	0.21	0.22
No. of Comparators in Main Quantizer	16	4	4	4
No. of Comparators in Extra Quantizer	0	16	16	16
Total No. of Comparators	16	20	20	20

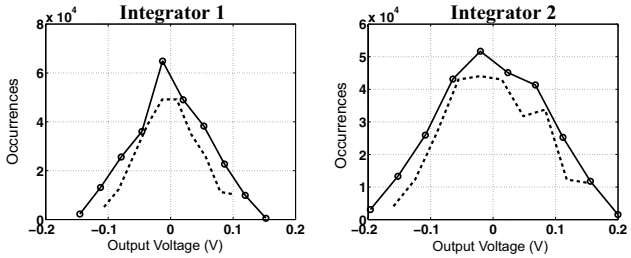

Fig. 7. Signal swing at the integrator outputs.
Here: _o_ proposed DFF ΔΣ modulator in Fig. 6 with K=1.
----- AFF ΔΣ modulator in Fig. 2b [2,4].

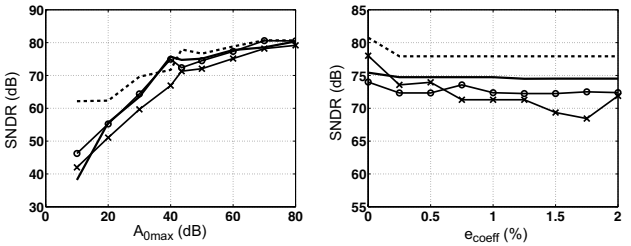

Fig. 8. SNDR versus:
a) opamp's maximum DC gain $A_{0\max}$ (with e_{coeff} = 1%);
b) modulator's coefficient error e_{coeff} (with $A_{0\max}$ = 150V/V).
Here: _o_ proposed DFF ΔΣ modulator in Fig. 6 with K = 1.
_x_ proposed DFF ΔΣ modulator in Fig. 6 with K = 2.
_ _ _ AFF ΔΣ modulator in Fig. 2b [2,4].
____ DFF ΔΣ modulator in Fig. 3 [5].

Observe that the sensitivity of the ΔΣ modulator to the finite dc gains of the opamps and to the variations in loop-filter coefficients (Table I and Fig. 8) is reduced by designing the proposed DFF modulator with K = 1, rather than K = 2 (Fig. 6). This performance improvement is a result of the 1st-order shaping ($1-z^{-1}$) of the quantization-noise leakage at the modulator output, when K=1 (as discussed in Section III).

V. CONCLUSION

A technique for designing DFF ΔΣ modulators with unity-gain STF was presented. A 2nd-order DFF ΔΣ modulator with unity-gain STF was proposed. Its performance (in terms off reduced signal swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, and robustness to modulator coefficient variations) were demonstrated and compared to previously-developed AFF and DFF ΔΣ modulators.

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