Digitally-Enhanced High-Order ΔΣ Modulators

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Abstract --- The input feedforward path in a ΔΣ modulator is an attractive technique for low-distortion swing-reduction design. It helps lower the power dissipation, especially in ΔΣ modulators designed with low oversampling ratios (OSRs) in low-voltage nanometer CMOS technologies. However, a ΔΣ modulator with analog feedforward (AFF) requires an analog adder before the quantizer, which can limit the achievable resolution or degrade the signal swing and increase the power dissipation. In this paper, a single-stage multibit ΔΣ modulator with digital feedforward (DFF) is proposed to realize a high-order finite-impulse-response noise transfer function, thereby achieving high signal-to-quantization-noise ratios at low OSRs. Its key features include reduced swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, and robustness to ΔΣ modulator coefficient variations, all of which are achieved using only minimal additional digital hardware. Behavioral simulation results confirm that the proposed DFF modulator achieves the swing-reduction and low-distortion performance of an AFF modulator, while eliminating the need for an analog adder.

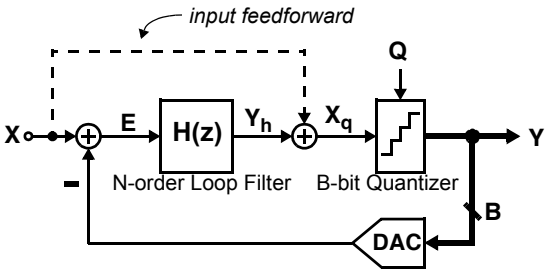
I. Introduction

The proliferation of broadband digital-communication applications is stimulating research towards the development of analog-to-digital converters (ADCs) with higher speeds and higher resolutions. Potential applications include high-speed wireless systems, such as 3G and 4G mobile terminals [1]. These high-speed high-resolution ADCs must be designed in standard digital CMOS processes to achieve higher system integration and lower fabrication costs, while harnessing the advanced digital-signal-processing capabilities of scaled CMOS processes. However, in nanometer CMOS technologies, the low-power design of high-resolution analog circuits is complicated by the low supply voltages and the small devices with poor analog-signal processing capabilities.

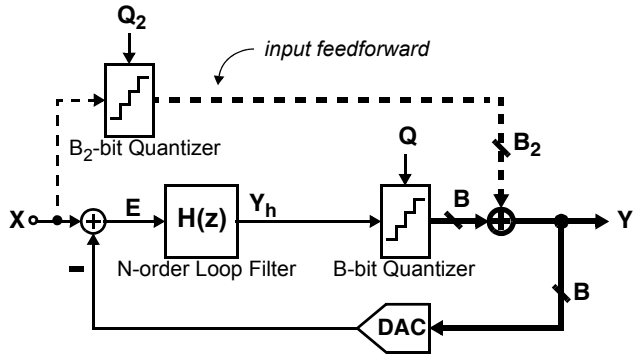
Oversampled ΔΣ ADCs are well known for their ability to achieve high-resolution A/D conversion in low-to-medium speed applications [2]. However, extending a ΔΣ ADC to broadband applications requires lowering its oversampling ratio (OSR) in order for its ΔΣ modulator to be realizable within the technology limitations of CMOS processes, while meeting a moderate power budget. Unfortunately, this limits the efficiency of a ΔΣ ADC in achieving high-resolution A/D conversion.

This paper explores several aspects of the design of high-speed high-resolution ΔΣ ADCs when the OSR and the supply voltages are limited by the CMOS technology. Namely:

1) High-Order Multibit ΔΣ Modulator: In a single-stage ΔΣ modulator (Fig. 1), the loss in signal-to-quantization-noise ratio (SQNR) due to OSR lowering can be compensated for by increasing the noise-shaping order N of the loop filter $H(z)$ and/or the resolution of the internal B-bit quantizer [2]. By fully exploiting the enhanced stability characteristics of multibit quantization (quantizer overload can be completely avoided [3]), a stable high-order ΔΣ modulator with an aggressive noise-transfer-functions (NTF) can be designed to achieve high SQNRs at low OSRs. Thus, the entire noise budget can be allocated to the analog-noise sources (mainly, thermal kT/C noise) to reduce the power dissipation.



(a) Analog-Feedforward (AFF) ΔΣ Modulator



(b) Digital-Feedforward (DFF) ΔΣ Modulator

Fig. 1. Linear model of a single-stage ΔΣ modulator with an input feedforward path (dashed line) implemented in: a) the analog domain; and b) the digital domain.

2) Input Feedforward Path: With an input feedforward path (dashed line in Fig. 1), the analog input signal no longer flows through the loop filter, but rather reaches the output through the feedforward path [3]. Since, ideally, the input signal is not processed by the opamps in the loop-filter integrators, no harmonic distortion is generated and the signal swing is reduced at the integrator outputs [4]. Hence, the input feedforward path in a ΔΣ modulator is an attractive technique for low-distortion swing-reduction design. It helps lower the power dissipation, especially for low-OSR ΔΣ modulators designed in a low-voltage nanometer CMOS technology [3].

The input feedforward can be implemented using either the analog feedforward (AFF) path in Fig. 1a or the digital feedforward (DFF) path in Fig. 1b. An AFF ΔΣ modulator with arbitrary-order NTF was presented in [3], whereas a DFF ΔΣ modulator with only a 2nd-order NTF was reported in [5].

In this paper, the advantages and design challenges of ΔΣ modulators with DFF versus AFF paths are outlined. Next, a general architecture for digitally-enhanced ΔΣ modulators is presented. Then, to enable the OSR reduction in high-speed ΔΣ ADCs without compromising the resolution, a multibit ΔΣ modulator with DFF is proposed to realize finite-impulse-response (FIR) NTFs of arbitrary orders. Its key features include reduced signal swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, robustness to ΔΣ modulator coefficient variations, all of which are achieved using only minimal additional digital hardware.

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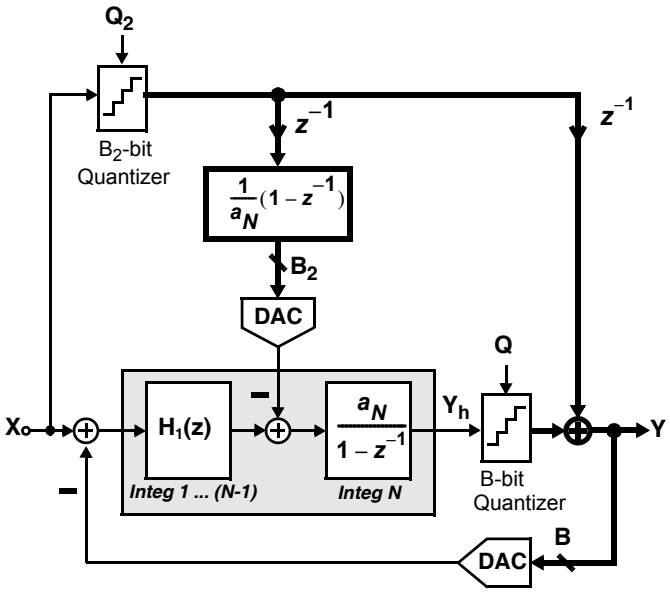


Fig. 2. Proposed architecture for a ΔΣ modulator with DFF.

This paper is structured as follows: Section II outlines the advantages and design challenges of DFF versus AFF ΔΣ modulators. Section III then proposes a multibit DFF ΔΣ modulator with an arbitrary-order FIR NTF. In Section IV, behavioral simulation results are presented to compare the performance of the proposed DFF ΔΣ modulator versus previously-reported AFF ΔΣ modulators.

II. Digital versus Analog Feedforward Path

A. Analog Implementation

The implementation of an AFF path is complicated by the need for an analog adder to realize the summation at the quantizer input (Fig. 1a). This analog adder can be implemented using:

a) an active analog summation amplifier [6]. However, since this analog amplifier must process the full-scale analog input signal, the signal swing at the modulator input will be limited by the available swing at the output of the analog amplifier. Furthermore, the need for active components (opamps) when using an active amplifier increases the overall power dissipation.

b) a passive switched-capacitor (SC) network [3]. This low-power solution is only effective when the number of quantization bits and, hence, the quantizer input capacitance is small. However, in the case of multibit quantization, a buffer is needed between the SC network and the quantizer for proper operation. Furthermore, to maintain the signal swing at the quantizer input, the quantizer reference voltage must be scaled down from its nominal value by a factor equal to the voltage drop across the passive SC network [3]. This also scales down (by the same factor) the quantizer step size and, hence, the minimum acceptable accuracy (maximum acceptable offset) for the comparators in the quantizer. Therefore, comparators with a higher resolution are required.

B. Digital Implementation

To overcome the drawbacks of an analog implementation, the input feedforward path can be implemented in the digital domain (Fig. 1b). This requires an extra quantizer. However, owing to the reduced signal swing with DFF (Section IV), the total number of comparators required in the main and the extra quantizers of a DFF ΔΣ modulator is actually smaller than that required in an AFF ΔΣ modulator with equivalent noise-shaping characteristics. Furthermore, although the extra quantizer injects additional quantization noise Q_2 at the modulator output, this paper presents a design technique to cancel Q_2 at the output of a DFF ΔΣ modulator (Section III).

III. Proposed ΔΣ Modulator with DFF

A. Proposed Architecture for a ΔΣ Modulator with DFF

Consider the ΔΣ modulator proposed in Fig. 2. Here, the input feedforward path is implemented in the digital domain. Then, to cancel the additional quantization noise Q_2 at the output of the DFF ΔΣ modulator, the output of the extra B_2-bit quantizer is differentiated in the digital domain and added to the input of the last integrator in the ΔΣ loop filter. This results in $-(X+Q_2)$ appearing at the modulator output, which cancels the $(X+Q_2)$ injected by the DFF path. Thus, the modulator output signal is:

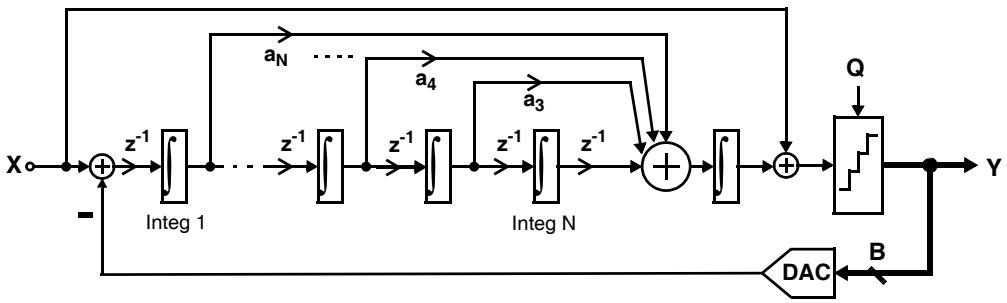
$$Y = STF \cdot X + NTF \cdot Q \tag{1}$$

where $STF = \dfrac{H}{1+H}$ Signal Transfer Function

$NTF = \dfrac{1}{1+H}$ Noise Transfer Function

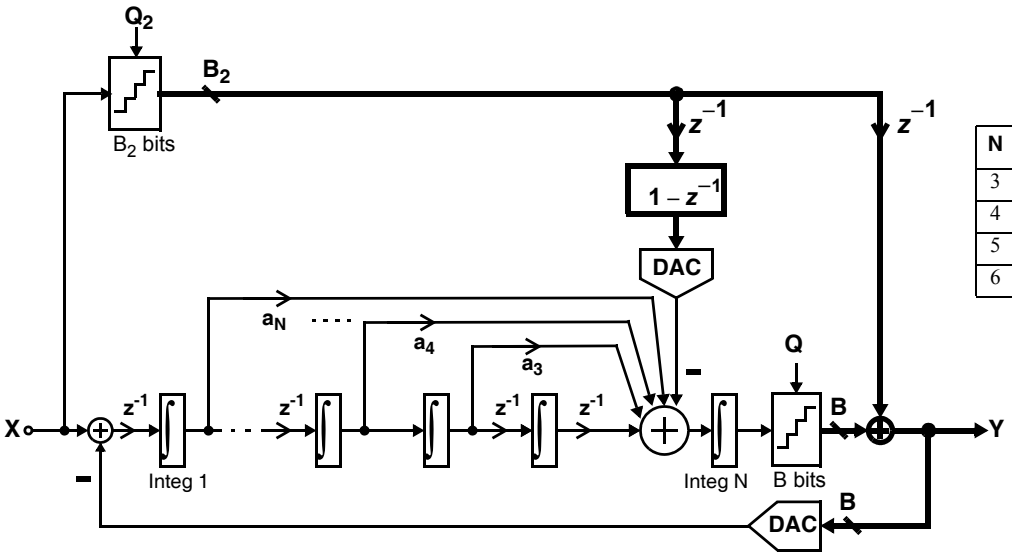
$H = H_1 \dfrac{a_N}{1-z^{-1}}$ *Loop Transfer Function*

This is identical to the output of a classical ΔΣ modulator with no input feedforward (Fig. 1a without the dashed line). However, the advantage of this DFF ΔΣ modulator is that the signal component at the output of the loop filter (the input of the main quantizer) is reduced from $STF \cdot X \cong X$ to $(STF - z^{-1})X \cong (1-z^{-1})X$ within the signal band. Thus, only the 1st derivative of the analog input signal X appears at the output of the last integrator in the ΔΣ loop filter. Accordingly, the signal swing is reduced at the output of the loop-filter integrators.



N	a_3	a_4	a_5	a_6
3	3			
4	$2 + 2z^{-1}$	4		
5	5	5	5	
6	4 and $2z^{-1}$	9	11	6

Fig. 3. A high-order ΔΣ modulator with AFF and an FIR NTF, presented in [3]. Here, $\int \equiv 1/(1-z^{-1})$.



N	a_3	a_4	a_5	a_6
3	3			
4	$2 + 2z^{-1}$	4		
5	5	5	5	
6	4 and $2z^{-1}$	9	11	6

Fig. 4. Proposed high-order multibit ΔΣ modulator with DFF.
The feedforward coefficients a_k ($k = 3, \ldots, N$) needed to realize the FIR NTF in equation (2) are given in the table. Here, $\int \equiv 1/(1 - z^{-1})$.

B. High-Order ΔΣ Modulator with DFF

The simplest NTF, which can achieve a high SQNR at low OSRs, is a high-pass FIR transfer function with N zeros at dc:

$$NTF = (1 - z^{-1})^N \tag{2}$$

To realize an FIR NTF of arbitrary order N, the multibit DFF ΔΣ modulator shown in Fig. 4 is proposed. This proposed design applies the DFF design concept shown in Fig. 2 to the AFF ΔΣ modulator shown in Fig. 3.

IV. Behavioral Simulation Results

A. Behavioral Simulation Conditions and Models

The proposed DFF ΔΣ modulator (Fig. 4) and the previously-reported AFF ΔΣ modulator (Fig. 3) were simulated in SIMULINK for the following design specifications:

- 3rd-order NTF (N=3) and OSR = 16
- 32-level mid-tread quantizer (B =5 bits).
- The quantizer reference voltage is normalized to $V_{\text{REF}} = 1$ V.
- The amplitude of the sinusoidal input is $V_{\text{in}} = 0.5$ V (-6 dBFS).
- The input-signal frequency is $f_{\text{in}} = f_S/(8 \cdot \text{OSR})$, in order for the first 4 input-signal harmonics to fall within the signal band.

The SIMULINK behavioral simulations accounted for the following loop-filter nonidealities:

1) Opamp Nonidealities: The discrete-time loop-filter integrators are modeled as described in [7] to account for the finite dc gains, the nonlinear dc-gain variations, and the output saturation voltages of the opamps in practical switched-capacitor (SC) integrators. These opamps are assumed to have a **maximum dc gain $A_{0\max}$** = 150 V/V (43 dB) and an output saturation voltage $V_{\text{Osat}} = 1$ V. This is to account for the low dc gains of the opamps in nanometer CMOS technologies. In these scaled technologies, opamps with low dc gains are readily obtainable using classical folded-cascode or current-mirror designs. However, high-gain opamps require either multiple gain stages or output-impedance enhancement [8], due to the low supply voltages and poor intrinsic gains of the MOS transistors in scaled CMOS technologies. Such gain-boosting techniques for the opamps significantly increase the power dissipation and degrade the speed.

2) Modulator Coefficients: To account for variations in modulator coefficients, the signal-to-noise-plus-distortion ratio (SNDR) values reported correspond to the minimum SNDR values found over 50 simulations in which each modulator coefficient is assumed to have a **uniformly-distributed random error** in the range $\pm e_{\text{coeff}} = 1\%$.

B. Behavioral Simulation Results

Table I summarizes the behavioral simulation results. Accordingly, the proposed DFF ΔΣ modulator achieves the same SNDR and output-swing reduction as the previously-reported AFF ΔΣ modulator. Observe that the signal swing at the quantizer input is much more reduced in the proposed DFF modulator, compared to the AFF modulator. This is because the inband signal component at the quantizer input is approximately X for the AFF modulator, whereas it is only $(1 - z^{-1})X$ for the proposed DFF modulator (Section III).

TABLE I Comparison between AFF and DFF ΔΣ Modulators

	AFF modulator [7] (Fig. 3) N = 3, B = 5 bits	**Proposed DFF modulator (Fig. 4)** N = 3, B = 5 bits	
		B_2 = 5 bits	**B_2 = 4 bits**
SNDR at $V_{\text{in}} = -6$ dBFS with $A_{0\max}$ = 150V/V, $\pm e_{\text{coeff}}$ = 1%	86.8 dB	86.5 dB	86.7 dB
1st-integrator Output Swing (absolute maximum)	0.12 V	0.11 V	0.11 V
2nd-integrator Output Swing (absolute maximum)	0.06 V	0.09 V	0.09 V
3rd-integrator Output Swing (absolute maximum)	0.19 V	0.21 V	0.23 V
Quantizer Input Swing (absolute maximum)	0.67 V	0.21 V	0.23 V
No. of Comparators in Main Quantizer	32	7	8
No. of Comparators in Extra Quantizer	0	32	16
Total No. of Comparators	32	39	24

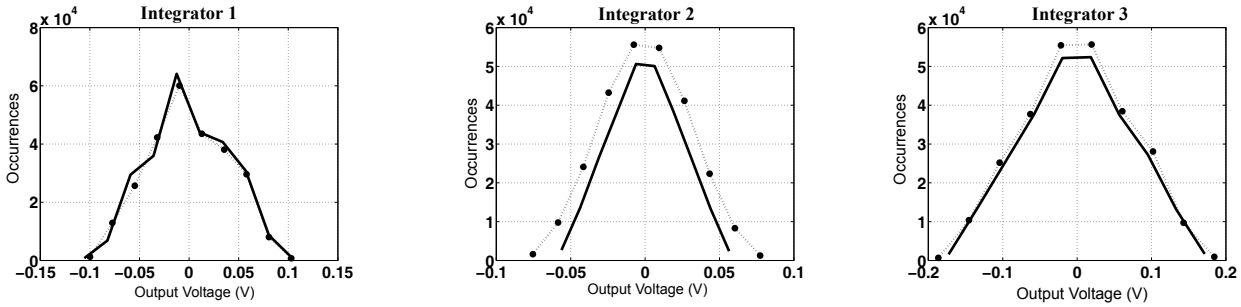


Fig. 5. Signal swing at the integrator outputs. Here: _•_ proposed DFF ΔΣ modulator in Fig. 4 (B = 5 bits, B_2 = 4 bits); ____ AFF ΔΣ modulator in Fig. 3 [5].

Thus, in the AFF modulator, the full-swing input signal X appears at the input of the main quantizer and, hence, all comparators in main quantizer are needed to digitize the input signal. However, in the proposed DFF modulator, only the 1st derivative of X appears at the input of the main quantizer. Owing to this swing reduction (as shown in Table I), the number of comparators needed in the main quantizer of the proposed DFF modulator can be reduced from 32 to $32 \times 0.21 \rightarrow 7$. Furthermore, observe that (Table I) the performance of the proposed DFF modulator is maintained even if the number of quantization bits B_2 in its extra quantizer is reduced from 5 bits (31 levels) to 4 bits (15 levels). Accordingly, the total number of comparators required in the main and the extra quantizers of the proposed DFF modulator is actually smaller than that required in the AFF modulator.

Figure 5 shows the swing distribution at the output of each integrator. Accordingly, the swing reduction in the proposed DFF ΔΣ modulator is comparable to that in the AFF ΔΣ modulator.

Figure 6a depicts the SNDR versus input-signal levels. Accordingly, the SNDR and dynamic-range performances of the proposed DFF modulator are similar to that of the AAF modulator.

Figure 6b shows the SNDR versus the maximum dc gain $A_{0\max}$ of the opamps, for a coefficient error e_{coeff} = 1%. Accordingly, the sensitivity of the proposed DFF modulator to nonlinear variations in opamp dc gains is comparable to that of the AFF modulator. Furthermore, it can achieve a high resolution and linearity (SNDR > 13 bits) using opamps with only moderate dc gains (as low as 60V/V or 36dB), thereby confirming the reduced sensitivity of the proposed DFF modulator to opamp dc gains.

Figure 6c shows the SNDR versus the error e_{coeff} in the modulator coefficients, assuming a maximum dc gain $A_{0\max}$=150V/V (43dB) for the opamps. Accordingly, the proposed DFF modulator can tolerate a 2% variation its loop-filter coefficients with only 1.1 dB drop in SNDR, thereby confirming the robustness of the proposed DFF modulator to coefficient variations.

V. Conclusion

A high-order multibit ΔΣ modulator with FIR NTF was proposed to reach high SQNRs at low OSRs. Through digital enhancement using minimal additional hardware, the proposed ΔΣ modulator achieves reduced swing at the opamp outputs, reduced sensitivity to integrator nonlinearities, and robustness to coefficient variations. Thus, it is particularly suitable for designing high-speed high-resolution ADCs in low-voltage CMOS technologies.

VI. References

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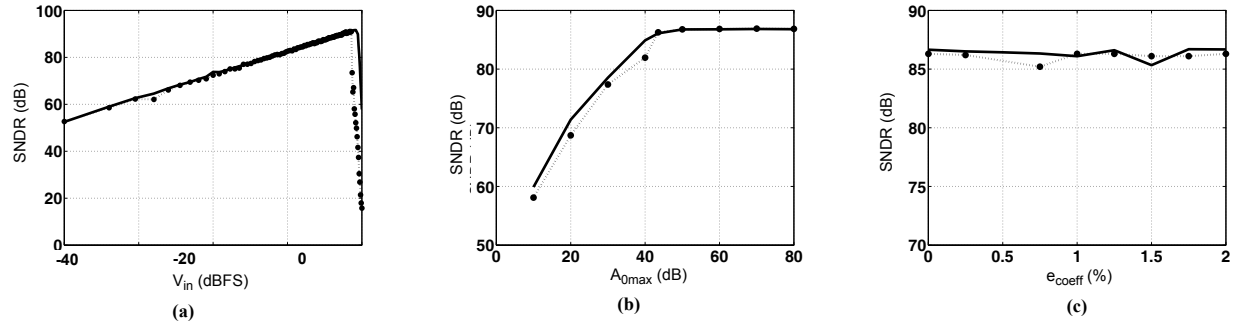

Fig. 6. SNDR versus: **a)** input-signal level V_{in} (with $A_{0\max}$ = 150V/V and e_{coeff} = 0); **b)** opamp's maximum DC gain $A_{0\max}$ (with e_{coeff} = 1%); and **c)** modulator's coefficient error e_{coeff} (with $A_{0\max}$ = 150V/V).

Here: _•_ proposed DFF ΔΣ modulator in Fig. 4 (N = 3, B = 5 bits, B_2 = 4bits); ____ AFF ΔΣ Modulator in Fig. 3 [5] (N = 3, B = 5 bits).