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Digital Background Calibration of a 0.4-pJ/step 10-bit Pipelined ADC without PN Generator in 90-nm Digital CMOS

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Abstract

In nanometer digital CMOS, the linearity of pipelined A/D converters (ADCs) is degraded by the low dc gains of the opamps. Gain-enhancement techniques significantly increase the analog-circuit design complexity at low power and low voltage. Therefore, even in medium-resolution applications, digital background calibration is attractive for designing power-efficient ADCs. A simple, yet accurate, digital background calibration technique, which does not require a pseudo-random (PN) calibration signal, is proposed to minimize the power dissipation in the digital calibration unit. It achieves the same convergence speed and accuracy as PN-based techniques in 2-path (split) pipelined ADCs. A 10-bit 44-MS/s pipelined ADC, fabricated in a standard 1.2-V 90-nm digital CMOS process, uses the proposed calibration technique to achieve a 58.7-dB SNDR for a 21.5-MHz input, with a figure-of-merit (FOM) of 0.4 pJ/step.

I. Introduction

The linearity of a pipelined analog-to-digital converter (ADC) is primarily degraded by linearity errors in its pipeline stages. In a switched-capacitor pipeline stage, the primary sources of linearity errors are: a) gain errors in the residue amplifier, due to the low dc gains of the opamps; and b) nonlinearity in the digital-to-analog sub-converter (sub-DAC), due to capacitor-mismatch errors.

For medium-resolution ($\leq$ 10 bits) pipelined ADCs, adequate capacitor matching is readily obtainable in standard nanometer CMOS processes. However, in these scaled processes, high dc gains for the opamps are not easily realizable at low power, due to the low supply voltages and the low intrinsic gains of the MOS transistors.

To design power-efficient pipelined ADCs in nanometer CMOS processes, one approach is to build high-gain opamps using: a) special high-performance analog transistors (however, this requires additional processing steps and, hence, higher fabrication costs) [1]; or b) analog gain-enhancement techniques (however, this increases the analog circuit-design complexity and the time-to-market) [2]. Another approach, followed in this paper, is to calibrate the pipeline stages for gain errors. Digital background calibration is the most attractive technique, as it is does not require high-resolution analog circuitry, it is portable across technologies and benefits from technology scaling, it is robust to environmental changes, and it does not interrupt the normal operation of the ADC. Although digital calibration is typically reserved for high-resolution applications, this paper demonstrates its power efficiency in the design of medium-resolution pipelined ADCs.

This paper describes a novel digital background calibration technique and its implementation in a 10-bit pipelined ADC with a split (2-path) architecture (Fig. 1). Fabricated in a standard 1.2-V 90-nm digital CMOS process, this ADC achieves a 58.7-dB SNDR (9.5-bit ENOB) for a 21.5-MHz input signal at a 44-MS/s sampling frequency, with a figure-of-merit of:

$$\mathrm{FOM} \equiv \mathrm{Power}/(2^{\mathrm{ENOB}} \cdot f_S) = 0.4 \text{ pJ/step}$$

Accordingly, it achieves a FOM comparable to the most power-efficient ADC [2], among the state-of-the-art 10-bit medium-speed ($\leq$ 200MS/s) pipelined ADCs fabricated in standard digital CMOS processes and measured at $f_{in} = f_S/2$ [2-8].

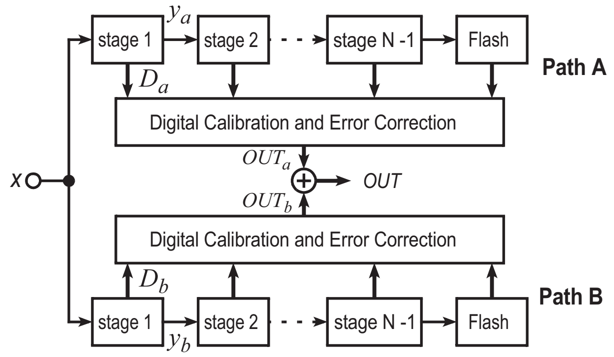

Fig. 1. Two pipelined ADCs, digitizing the same input signal and forming a 2-path ADC (paths *A* and *B*).

This FOM (low power) is achieved through:

1) Digital Background Calibration without PN Generator: Previously-reported techniques for digital background calibration have utilized either: a) a pseudo-random binary signal, referred to as a PN signal, to measure the ADC nonlinearity (which requires a PN-signal generator and extra analog and digital circuitry to inject the PN signal) [10,11]; or b) a high-precision low-speed reference ADC to calibrate the main pipelined ADC (which increases the analog design complexity, power dissipation, and chip area) [12,13].

To minimize the power dissipation of the digital calibration unit, this paper proposes a digital background calibration technique that uses a constant, rather than a pseudo-random (PN), calibration signal. The proposed technique is then utilized to calibrate the pipelined ADC prototype and is synthesized on a 90-nm FPGA to estimate the power dissipation of the digital calibration unit. In addition to the digital power savings achieved using the proposed calibration technique, the experimental results confirm that equivalent calibration convergence (accuracy and speed) are achieved using the proposed calibration technique (no PN generator), as using classical calibration methods (with PN generator) [10,11] in 2-path pipelined ADCs.

2) Low-Gain Opamps: Through digital calibration of gain errors, the dc-gain requirements on the opamps in the pipeline stages are relaxed. Thus, a classical two-stage opamp design with low dc gain and low power can be utilized.

The paper outline is as follows: Section II describes the pipelined ADC architecture. Section III proposes a digital background calibration technique for 2-path pipelined ADCs. Section IV presents the measured performance of the experimental pipelined ADC, including a comparison of its power dissipation to state-of-the-art designs and a comparison between its output convergence using the proposed and classical calibration techniques.

II. Pipelined ADC Architecture

Pipelined ADCs with a split (2-path) architecture (Fig. 1) have been demonstrated to significantly reduce the calibration time of PN-based calibration techniques, without increasing the chip area and power consumption compared to their classical (1-path) equivalents [10,11]. This paper assumes that the 1st pipeline stage in each path of the 2-path pipelined ADC is a 1.5-bit residue stage (Fig. 2).

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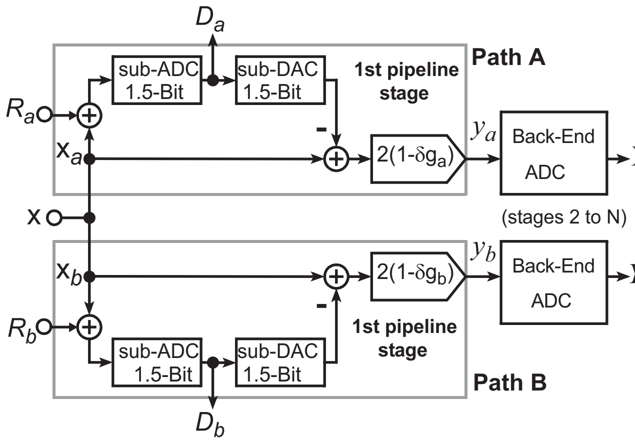


Fig. 2. The 2-path ADC in Fig. 1, with the 1st pipeline stage in each path designed as a 1.5-bit residue stage (1-bit effective resolution). Here, δg_a and δg_b are the gain errors in paths *A* and *B*, respectively. Signals R_a and R_b are added to calibrate the 1st pipeline stage in each path.

Calibration signals R_a and R_b are used to measure the gain errors in paths *A* and *B* (Fig. 2). Observe that the calibration signal in each path is added to the sub-ADC input, rather than the pipeline-stage input, such that it does not to limit the input-signal swing [10].

The inputs of the 1st pipeline stages in paths *A* and *B* will experience different offset and noise errors, due to the separate routing of the ADC input signal x to each path. Therefore, the input signals to paths *A* and *B* (Fig. 2) can be expressed as:

$$x_a = x + \Delta x_a + N_a \quad \text{and} \quad x_b = x + \Delta x_b + N_b \tag{1}$$

where Δx_a and Δx_b are offset errors, while N_a and N_b are zero-mean noise errors, added to the ADC input signal x in paths *A* and *B*, respectively. The residue signals of the 1st pipeline stages in paths *A* and *B* (Fig. 2) can then be expressed as:

$$y_a = (2x_a - D_a V_{\mathrm{ref}})(1 - \delta g_a) \tag{2}$$

$$y_b = (2x_b - D_b V_{\mathrm{ref}})(1 - \delta g_b) \tag{3}$$

where digits D_a and D_b (with values $\pm V_{\mathrm{ref}}$ or 0) are the sub-ADC outputs, while δg_a and δg_b are the gain errors. In the following, a unity reference voltage ($V_{\mathrm{ref}} = 1$) is assumed for simplicity.

III. Proposed Calibration Technique

A. Gain-Error Estimation

To simplify the calibration algorithm, assume that the 1st pipeline stages in paths *A* and *B* have the same gain error δg:

$$\delta g = \delta g_a = \delta g_b \tag{4}$$

This is a reasonable assumption, as most of the gain error is due to the low dc gains of the opamps in the pipeline stages and both paths use the same opamp design. The validity of this assumption will be verified experimentally (Section IV).

Constant dc signals R_a and R_b can be added (Fig. 2) to create a mismatch between the transfer functions of paths *A* and *B*. Figure 3 depicts the input-output transfer functions of the 1st pipeline stages in paths *A* and *B*, when:

$$R_a = 1/8 \text{ and } R_b = -1/8 \tag{5}$$

It can be shown that these constant signals do not affect the ADC functionality, if $|R_a|$ and $|R_b|$ are less than 1/4 [10].

Assume that the residue signals y_a and y_b are perfectly digitized as Y_a and Y_b by the subsequent pipeline stages in Fig. 1 (the back-end ADCs in Fig. 2). Then:

$$Y_a = (2x_a - D_a)(1 - \delta g) + \Delta y_a \tag{6}$$

$$Y_b = (2x_b - D_b)(1 - \delta g) + \Delta y_b \tag{7}$$

where Δy_a and Δy_b are offset errors, due to the 1st pipeline stage and the back-end ADC in paths *A* and *B*, respectively.

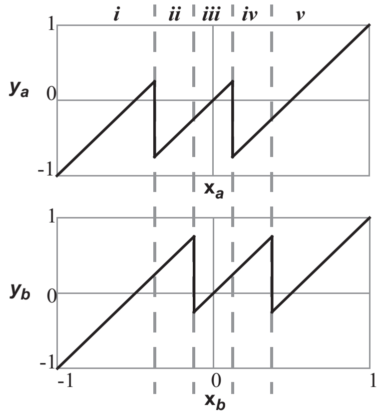


Fig. 3. Input-output transfer curves of the 1st pipeline stages in paths *A* and *B* in Fig. 2, when R_a=1/8 and R_b=-1/8.
The corresponding sub-ADC output digits are:
D_a= -1 (region *i*), 0 (regions *ii* and *iii*), 1(regions *iv* and *v*)
D_b= -1 (regions *i* and *ii*), 0 (regions *iii* and *iv*), 1 (region *v*)

Then:

$$Y_b - Y_a = [2(x_b - x_a) - (D_b - D_a)](1 - \delta g) + (\Delta y_b - \Delta y_a) \tag{8}$$

Step 1 When $D_a = D_b$:

This corresponds to regions *i*, *iii*, and *v* of the pipeline-stage transfer curves in Fig. 3, where $D_a - D_b = 0$. Therefore, equation (8) simplifies to

$$Y_b - Y_a = 2(x_b - x_a)(1 - \delta g) + (\Delta y_b - \Delta y_a) \tag{9}$$

Define a signal error E as the average of $Y_b - Y_a$.
Then, substituting (1) into (9) and taking the average:

$$E \equiv \overline{Y_b - Y_a} = 2(\Delta x_b - \Delta x_a)(1 - \delta g) + (\Delta y_b - \Delta y_a) \tag{10}$$

The signal error E will be used to estimate gain error δg.

Step 2 When $D_a \neq D_b$:

This corresponds to regions *ii* and *iv* of the pipeline-stage transfer curves in Fig. 3, where $D_a - D_b = 1$. Therefore, equations (6), (7), and (10) can be combined and simplified to:

$$(Y_b - Y_a) - E = [2(N_b - N_a) + 1](1 - \delta g) \tag{11}$$

Taking the average of equation (11) leads to:

$$\overline{(Y_b - Y_a) - E} = 1 - \delta g \tag{12}$$

Therefore, the gain error can be estimated as:

$$\delta g = 1 - \overline{(Y_b - Y_a) - E} \tag{13}$$

B. Gain-Error Correction

A non-zero gain error δg affects the digitized residue signals Y_a and Y_b, as per equations (6) and (7). Let $Y_{a,\mathrm{cal}}$ and $Y_{b,\mathrm{cal}}$ denote the calibrated values of Y_a and Y_b, with the effect of δg removed. Assuming $\delta g^2 \ll \delta g$, these can be computed in the digital domain as:

$$Y_{a,cal} = Y_a(1 + \delta g) \quad \text{and} \quad Y_{b,cal} = Y_b(1 + \delta g) \tag{14}$$

These calibrated residue signals are then passed to the digital error-correction block, which generates the ADC output.

C. Summary of Calibration Steps

Figure 4 summarizes the proposed digital background calibration algorithm for the 2-path ADC (Fig. 2):

- When $D_a = D_b$, update signal error E, using equation (10).
- When $D_a \neq D_b$, update gain error δg, using equation (13).
- Digitally calibrate residue signals Y_a and Y_b, using equation (14).
- Pass the calibrated residue signals $Y_{a,\mathrm{cal}}$ and $Y_{b,\mathrm{cal}}$ to the digital error-correction block to compute the ADC output.

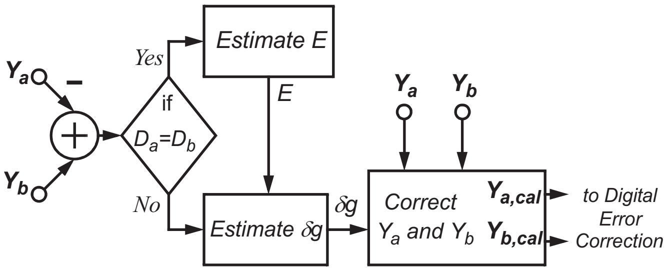


Fig. 4. Proposed digital background calibration algorithm.

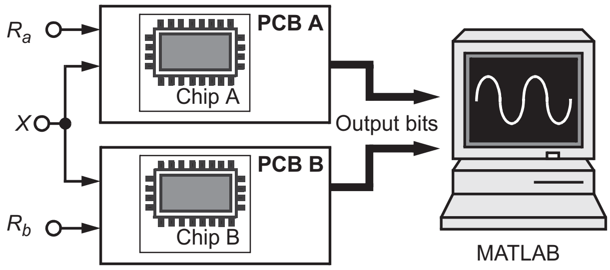


Fig. 5. Test setup for the 2-path ADC, with two ADC chips (*A* and *B*) connected to form the 2-path ADC.

D. Comparison to PN-based Digital Calibration Techniques

Compared to previously-reported PN-based methods for the digital background calibration of 2-path pipelined ADCs [10,11], the proposed technique differs as follows:

1) *Calibration Signals R_a and R_b*: In PN-based methods, R_a and R_b are two different pseudo-random (PN) binary signals. This requires a PN-signal generator and additional analog and digital circuits to apply the time-varying PN signals to the pipeline stages. Using the proposed calibration technique, this extra circuitry is not required, as the calibration signals have constant dc values ($R_a = 1/8$ and $R_b = -1/8$).

2) *Gain Errors δg_a and δg_b*: In PN-based calibration methods, the gain error is calibrated separately for each path. In the proposed calibration technique, the gain errors are assumed to be equal in both paths ($\delta g = \delta g_a = \delta g_b$) for simplicity. The validity of this assumption will be verified experimentally under worst-case conditions (Section IV).

IV. Experimental Results

The proposed calibration technique is implemented in a 2-path pipelined ADC. Each path is a 10-bit pipelined ADC, consisting of eight 1.5-bit pipeline stages followed by a 2-bit flash ADC. As the ADC performance is most sensitive to the 1st pipeline stage in each path, only these stages are calibrated.

Owing to the digital gain calibration, the dc-gain requirements are relaxed on the opamps in the pipeline stages. Hence, the opamps are designed using a simple two-stage configuration (which has a good noise performance, simple biasing, and large output-voltage swing). Furthermore, owing to the digital error correction, the offset requirements are relaxed on the comparators in the sub-ADCs of the pipeline stages. Hence, the implemented design uses dynamic comparators.

A. Experimental Test Setup

One path of the 2-path pipelined ADC has been fabricated in a standard 1.2-V 90-nm digital CMOS process (Fig. 10). To realize the 2-path ADC, two ADC chips are then mounted on two identically-designed PCBs (Fig. 5). Both PCBs are then driven by the same analog-input and clock signals, but with calibration signals R_a and R_b applied to PCBs *A* and *B*, respectively. The proposed calibration technique is implemented in MATLAB.

By fabricating only one path of the 2-path ADC and utilizing this experimental test setup (Fig. 5), significant savings in chip area and, hence, fabrication cost are achieved for the ADC prototype. Furthermore, by implementing each path on a different die, the worst-case mismatch between gain errors δg_a and δg_b is present. This allows us to experimentally verify our hypothesis (equation (4)) that gain errors δg_a and δg_b can be assumed equal for the purpose of gain calibration, even under worst-case matching conditions.

B. Dynamic and Static Performance

Figure 6 shows the output spectrum of the calibrated 2-path ADC for a 21.5-MHz input signal sampled at 44 MS/s. The SNDR is 58.7 dB (9.5-bit effective resolution). The 3rd-order harmonic is below -68 dB, resulting in a 68-dB SFDR.

Figure 7 shows the measured SNDR of the 2-path ADC versus input-signal frequency, with and without calibration. The sampling frequency is 44 MS/s. Accordingly, the SNDR is improved by 4dB, using the proposed calibration technique.
Furthermore, an SNDR of more than 58 dB is achieved across the full input-frequency range (250 kHz - 21.5 MHz).

Figure 8 shows the INL and DNL of the calibrated 10-bit 2-path ADC, sampled at 44 MS/s. The INL and DNL are less than 1 LSB and 0.8 LSB, respectively.

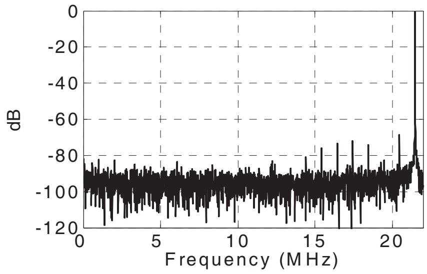


Fig. 6. Output spectrum after calibration, for a 21.5-MHz input signal sampled at f_S = 44 MS/s.

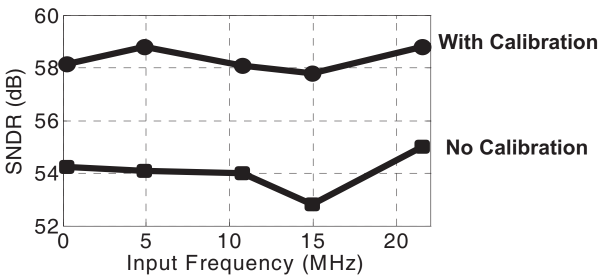


Fig. 7. Measured SNDR vs. input-signal frequency, sampled 44 MS/s.

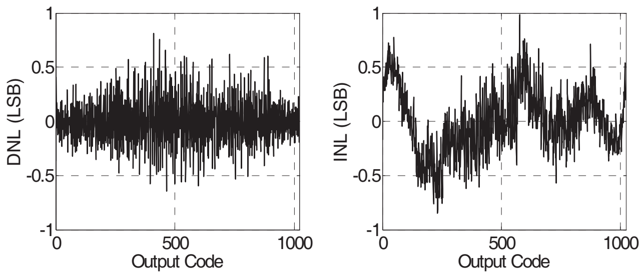
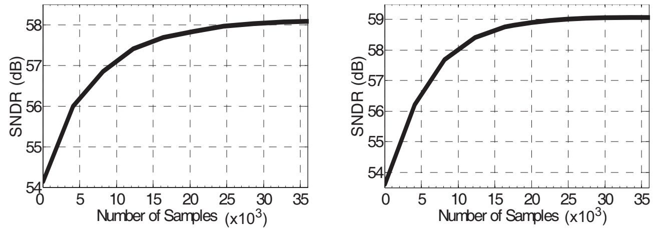


Fig. 8. DNL and INL after calibration, at 44-MS/s sampling frequency.



(a) Proposed Calibration **(b) Classical Calibration [2,3]**

Fig. 9. SNDR values during the normal ADC operation, using:
(a) Proposed calibration technique (with R_a=1/8 and R_b=-1/8);
(b) Classical PN-based calibration [10,11] (where R_a and R_b are two uncorrelated PN binary signals).

C. Convergence Accuracy and Speed

In our ADC prototype chip, calibration signals R_a and R_b were made available off-chip, in order to test calibration techniques with different R_a and R_b. Figure 9 compares the convergence speed of the proposed calibration technique (with $R_a = 1/8$ and $R_b = -1/8$) and the previously-reported PN-based calibration technique in [10-11] (where R_a and R_b are two uncorrelated PN binary signals). Accordingly, both techniques show the same convergence speed, requiring about 10^4 samples to converge to within 1dB of the final SNDR. Furthermore, the final SNDR values reached using both techniques are within 1dB. This confirms that the proposed calibration technique achieves the same performance (convergence speed and accuracy) compared to previously-reported PN-based methods, while being simpler to implement (Section III).

D. Power Dissipation

To estimate the power dissipation when using the proposed digital calibration technique, the digital calibration unit has been synthesized on an FPGA (EP2C5T144C6, Syclone II, 90 nm, 1.2 V). Its power consumption is estimated to be 3.1 mW, for a 1.4-Vpp 21.5-MHz sinusoidal signal at the 2-path ADC input and a 44-MS/s sampling frequency. Table I summarizes the ADC performance specifications.

Medium-speed (≤ 200MS/s) 10-bit pipelined ADCs with FOM < 0.8pJ/step have been proposed for applications ranging from wireless area networks to digital video broadcast [1-9]. Table II compares the performance of these ADCs, with the comparison limited to the ADCs fabricated in standard digital CMOS processes and their performance measured at $f_{in} = f_S/2$ [2-8]. Thus, this work achieves a FOM comparable to the most power-efficient ADC [2], among these state-of-the-art 10-bit medium-speed pipelined ADCs.

V. Conclusion

A simple, yet accurate, digital background calibration technique was proposed to minimize the power dissipation in the digital domain (by using constant, rather than pseudo-random, calibration signals) and the analog domain (by relaxing the requirements on the opamp dc gains) of 2-path pipelined ADCs. A 10-bit 44-MS/s ADC, fabricated in a standard 1.2-V 90-nm digital CMOS process, was presented to experimentally demonstrate the efficiency (in terms of energy per conversion step) of using the proposed calibration technique for the design of medium-resolution medium-speed pipelined ADCs in standard nanometer digital CMOS processes.

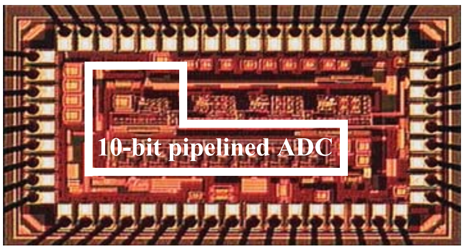


Fig. 10. Die micrograph in 90-nm standard digital CMOS technology.

TABLE I Measured Performance Summary

Technology	90-nm standard digital CMOS
Voltage Supply	1.2 V
Full-Scale Analog Input	1.4 V_{pp}
Resolution	10 bits
Sampling Rate (f_s)	44 MS/s
INL	1 LSB
DNL	0.8 LSB
SFDR @ f_{in}=21.5MHz	68 dB
SNDR @ f_{in}=21.5MHz	58.7 dB (9.5 bits)
Analog Power @ V_{DD} = 1.2 V	8 mW
Digital Power @ V_{DD} = 1.2 V	4.2 mW
FOM = Power/($2^{\text{SNDR in bits}}$.f_S)	0.4 pJ/step

TABLE II Performance Comparison of 10-bit Pipelined ADCs, measured at f_{in}=f_S/2 in standard digital CMOS.

Ref.	CMOS (nm)	V_{DD} (V)	f_s (MHz)	Power (mW)	SNDR (dB)	Calibrate	FOM (pJ/step)
ISSCC05 [8]	180	1.8	125	40	53.7	No	0.79
ISSCC05 [7]	90	1.2	12	3.3	52.6	No	0.76
ISSCC06 [6]	90	1.2	100	35	56.7	No	0.6
JSSC07 [5]	90	1	100	33	55.3	No	0.69
JSSC06 [4]	90	1.2	200	54.6	53.6	No	0.7
JSSC07 [3]	180	1.8	50	11	54.6	No	0.5
ISSCC07 [2]	90	1.2	80	13.3	55.6	No	0.34
This work	90	1.2	44	12.2	58.7	Yes	0.4

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