Epileptic Low-Voltage Fast-Activity Seizure-Onset Detector

Muhammad Tariqus Salam[1], Mohamad Sawan[1], Dang Khoa Nguyen[2], and Anas A. Hamoui[3]
[1]Polystim Neurotechnologies Laboratory, École Polytechnique de Montréal, Québec
[2]Department of Neurology, Centre Hospitalier de l'Université de Montréal, Québec
[3]Department of Electrical Engineering, McGill University, Montréal, Québec
tariqus.salam@polymtl.ca

Abstract – **In this paper, we present a seizure detector that is part of an implantable CMOS integrated device intended to identify seizure onsets and trigger focal treatment to disrupt seizure progression. The detector consists of a preamplifier, voltage level detectors, digital demodulators and a high-frequency detector. Variable gain amplification, adjustable threshold voltage identification and tunable recognition of high-frequency activities provide unique detection criteria for a specific patient. Moreover, digitally-controlled low-power CMOS circuits perform accurate seizure detection. A mathematical model of the seizure detection algorithm was validated in Matlab and circuits were implemented in a CMOS 0.18-µm process. Total power consumption of the detector is 6.71 µW. Detection performance was verified using intracerebral electroencephalographic recordings from a patient with epilepsy.**

I. Introduction

Approximately 50 million people in world have epilepsy, a third of whom are refractory to antiepileptic drugs. Many of the latter are not good epilepsy surgery candidates or have continued to have seizures despite surgery. Thus, novel therapeutic options for refractory epilepsy are needed. Over the last few years, there has been growing interest in the development of implantable epilepsy therapy devices. So far, the vagus nerve stimulator (VNS) is the only Food and Drug Administration (FDA) approved medical device for the treatment of epilepsy. However, less than 3% obtain seizure-freedom and only 30 to 40% show a reduction in seizure frequency of more than 50% with this scheduled (open-loop) stimulation device. Neuropace, a cranially implanted responsive neurostimulator triggered by seizure detection, is currently undergoing clinical evaluation.

Drug-resistant epileptics usually suffer from partial epilepsy. Seizures originate from a focal epileptogenic zone frequently spreading to adjacent regions. Electrographically, several patterns can be seen at seizure onset, depending on such factors as etiology, location, position of intracerebral electrodes. The most common seizure patterns are the low-voltage fast-activity, the high-voltage fast-activity or the rhythmic spiking [1]. Clinically, these ictal discharges usually lead to a variety of behavioral manifestations but may also be clinically silent (i.e. electrical seizures) especially if the ictal discharge remains very focal (without spread), is brief (few seconds) and occurs in non-eloquent cortex.

Many seizure prediction algorithms have been proposed so far via accumulation of energy [2], percentile tracking filter [3] and pattern recognition [4]. These algorithms are developed using high speed computer for short-term applications. However these types of algorithms cannot be employed in a low-power implantable microchip. The intracerebral electroencephalographic (EEG) recording with the intracranial electrodes is generally characterized by low-amplitude signal (microvolts) and low-frequency bandwidth. This neural signal represents synchronous firing of many neurons throughout a region across the diameter of an electrode contact. Due to the microvolt-level range, the neural signal must be amplified very carefully before further analysis (e.g. detection, digitization). Because CMOS technology has relatively poor noise performance, the low-amplitude amplification requires a CMOS amplifier with low input-referred noise. However, the restrictions on power consumption and size of an implantable device limits increasing the biasing current; therefore, design trade-offs between the biasing current and noise are required to optimize the performances of a device.

This paper presents a low-power low-noise CMOS seizure onset detector for the treatment of epilepsy. The proposed method uses the specific features of a patient in order to detect his/her seizure onset. This method is applicable for all patients who have the common seizure onsets characterized by progressive increase of low-voltage fast-activity in intracerebral EEG recordings. Thus, an adjustable gain of amplifier can emphasize the amplitude level of interest, and variable threshold voltages of a voltage level detector delimits the detected signals' locations and extracts the information of frequency as well as progressive increase in amplitude. Tuneability of the high frequency detector facilitates accurate detection of the seizure frequency of a patient. However, because the low-voltage amplification could cause degradation of input signal due to flicker noise, the detector performs analog signal processing by imposing input signal into high frequency and demodulation of the signal takes place in digital domain. As a result, overall input referred noise and power consumption are reduced. This detection is expected to be highly reliable in an implantable device without risking false detections of physiological rhythms (e.g. sleep spindle).

II. Detection Algorithm

Due to the high sensitivity of intracerebral EEG recordings and occasional electroclinical seizures, the acquisition system records abundant interictal epileptic spikes and brief electrical seizures (ES). Furthermore, ictal patterns vary from patient to patient according to the underlying substrate, the type of intracerebral electrodes used and their location according to the epileptogenic zone. For these reasons, the seizure detection algorithm requires several adjustable parameters to avoid false detection of normal rhythms, asymptomic interictal spikes and unharmful brief electrical seizures. This would erroneously trigger unwarranted focal treatment and deplete the battery life.

Fig. 1 shows the intracerebral EEG recording of brief electrical seizures followed by an electroclinical seizure. The recording is initially analyzed in Matlab software and a seizure detection algorithm for partial-onset seizures is proposed.

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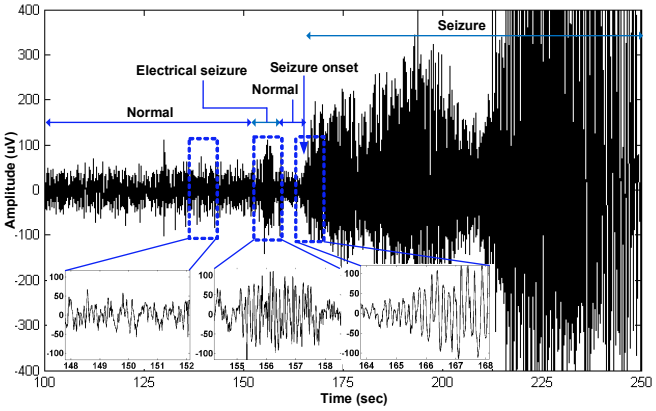

Fig. 1. Invasive EEG recordings of a patient with refractory focal epilepsy; zoom insets show normal activity, an electrical seizure and the onset of an electroclinical seizure characterized by low-voltage fast-activity.

In this algorithm, the input signal is modulated into high frequency ($F_s = 1/T_s$) so that instrumentation low-frequency noise does not affect the signal. The discrete modulated signal (V_{MOD}) confined to a time frame (T_f) passes through N number of voltage level detectors (VLD) to detect the specific features characterized by progressive hyperexcited signal. Threshold voltages of VLD ($V_{iHET1,2}$) and T_f are tuned to the specific seizure onset frequency (f_{STH}) of a patient so that no false alarms happen during a seizure detection. The following Eq. (1) shows that the seizure frequency is defined by the total number of identified pulses (V_{Di}) in VLDs confined to T_f.

$$f_{SZi} = \frac{\sum_{n=1}^{T_f/T_s} V_{D_i}(n)}{T_f} \tag{1}$$

where, i =1, 2, 3, ….., N. Thus, seizure onset will be declared based on following conditions (Eq. (2)).

$$V_{SB}(n) = \begin{cases} '1', & Seizure,\ f_{szi} > f_{STH} \\ '0', & No\ \ Seizure,\ otherwise \end{cases} \tag{2}$$

Fig. 2 demonstrates the seizure detection algorithm on the different patterns (e.g. (a) normal, (b) electrical seizure and (c) electroclinical seizure) of Fig. 1. These signal patterns are modulated (Fig. 2 (d) - (f)) and each of these modulated signals passes through six VLDs (threshold voltages are

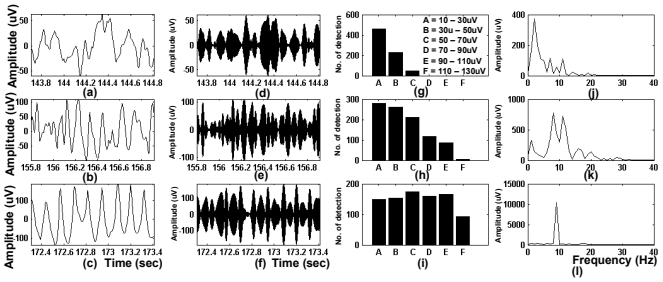

Fig. 2. Detection of epileptic seizure onset in Fig. 1: (a) normal signal; (b) electrical seizure, (c) clinical seizure; (d)-(f) are modulated signals (V_{MODi}) of (a)-(c) respectively; (g)-(i) are output of VLDs (V_{SDi}); (j)-(l) frequency analysis of the signals (a)-(c).

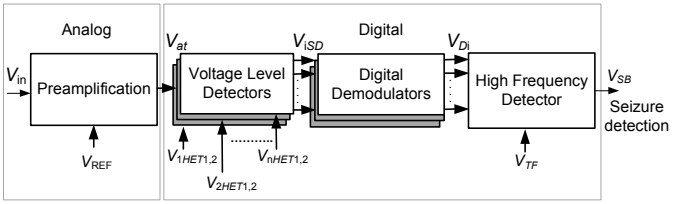

Fig. 3. Block diagram of the proposed detector.

shown in Fig. 2(g)). The high numbers of detection in Fig. 2 (g) - (i) represents high frequency and the similar numbers of detection represents progressive increases of these signals. Fig. 2 (j) - (l) shows frequency analysis of these signal patterns. Finally, this algorithm can able to determine the high frequency as well as progressive increases in amplitude (Fig. 2(i)) of the seizure signal and avoid the false alarm due to the three second high frequency ES (Fig. 2(k)).

III. Proposed System

The functional block diagram (Fig. 3) presents the architecture of the seizure onset detector (SOD). This detector consists of a preamplifier, voltage level detectors (VLD), digital demodulators (DD) and a high frequency detector (HFD). In this SOD, several variable parameters (V_{REF}, $V_{iHET1,2}$ and V_{TF}) are introduced to facilitate high accuracy in real-time seizure onset detection. In Fig. 3, V_{REF} controls the amplification of signal, the threshold voltages $V_{iHET1,2}$ are variable in VLD and V_{TF} sets the desirable frequency in HFD. Most of the signal processing in the SOD is accomplished in the digital domain, because of the relatively poor noise performance of CMOS technology. In Fig. 3, the preamplifier modulates at first the neural signal in F_s and amplifies the input amplitude level of interest. Subsequently, the VLDs convert the amplified signal (V_{at}) to a digital signal (V_{iSD}). Once the V_{at} is converted to a digital signal V_{iSD} , there is no further possibility to add noises in this signal. Then the V_{iSD} is demodulated to the original digital signal (V_{Di}). Finally, the HFD detects the seizure onset frequency of the patient and declares a warning (V_{SB}) without false alarm. Details of the SOD are described below.

IV. Circuit Implementation

As illustrated in Fig. 3, the SOD comprises four functional blocks. Details are given below.

A. Preamplification

A new chopper stabilized preamplification method was introduced in our previous work [5], where the demodulator and low-pass filter of a classical chopper stabilized preamplifier [6] was replaced by a high-pass filter. This preamplifier is advantageous over the classical preamplifier, because a demodulator adds further noise (ripple noise) and a low-pass filter with sharp cutoff frequency consumes extra power. In our design, a band-limited preamplifier modulates the input signal in F_s frequency and attenuates thermal noise V_{nt}. In this preamplifier, a high-pass filter comprises a capacitor and two PMOS transistors that attenuate various amplifier noises (e.g. flicker noise V_k and dc offset voltage noise V_{os}). Overall, the new preamplifier (Fig. 4(a)) has lower power consumption (6.70 µW) and improved input-referred noise (6 µVrms) in 17 kHz (2 kHz to 19 kHz) bandwidth.

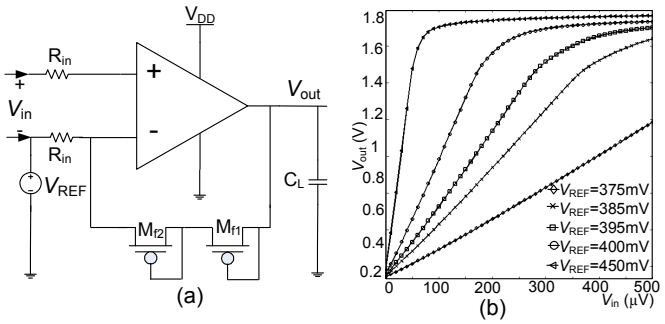

Fig. 4. Preamplification front-end: (a) is neural amplifier, (b) demonstrates variable gain of the amplifier with changing of V_{REF}.

Moreover, the variable gain of the amplifier can emphasize certain amplitude range of the neural signal (Fig. 4(b)).

B. Voltage level detector (VLD)

A VLD consists of comparators, logic gates, master salve DFF and a buffer. A low-power comparator includes two cascaded CMOS inverters [7], with the threshold voltage set by the aspect ratios of the transistors. The main disadvantage of this comparator is the fixed threshold voltage in an integrated device. However, a modified version of the comparator (Fig. 5(a)) provides variable threshold voltage (V_{HETi}).

$$V_{HETi} = \frac{V_{DD} - V_{SGp1} - |V_{tp}| + V_{tn}\sqrt{K_n / K_p}}{1 + \sqrt{K_n / K_p}} \qquad (3)$$

where, V_{tp} and V_{tn} are the threshold voltage of the NMOS and PMOS device, respectively; V_{SGp1} is the source to gate voltage of Mcp1 transistor; and $K_n = (W/L)_n\, \mu_n\, C_{ox}$ and $K_p = (W/L)_p\, \mu_p\, C_{ox}$. Eq. (3) shows that V_{SGp1} is the only variable parameter that can adjust the value of V_{HETi} in an integrated circuit. Fig. 5 (b) depicts the variation of V_{SGP1} with V_{STHi} and the corresponding changes of the V_{HETi} are shown in Fig. 5 (c). The other advantages of the modified comparator are no static power consumption, no hysteresis effect and relatively small transistor area.

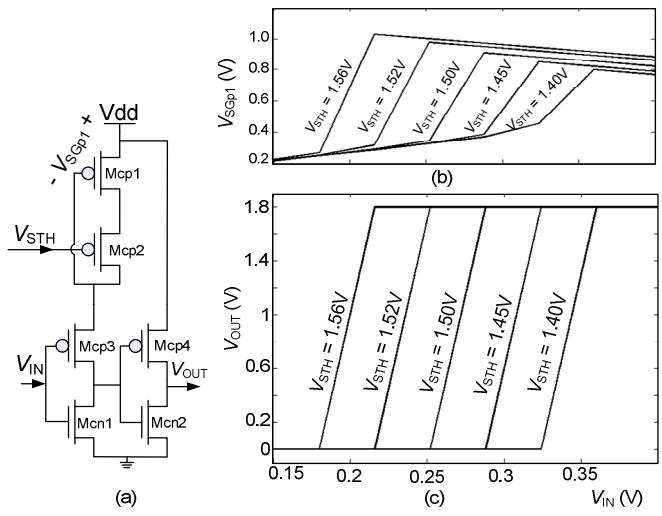

Fig. 5. A modified comparator: (a) schematic diagram of a comparator, (b) The variation of V_{SGp3} with different V_{STHi} and (c) DC swiping of the comparator for the different values of V_{STHi}.

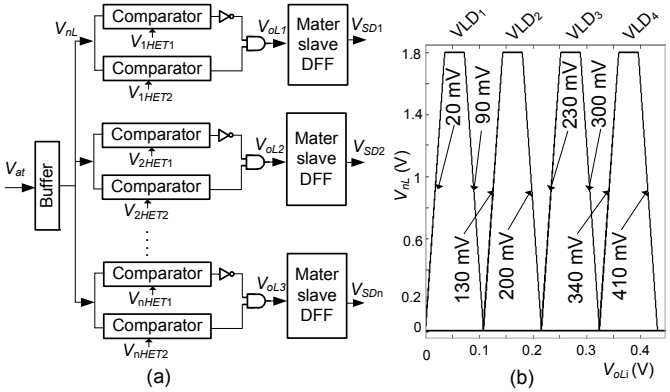

Fig. 6. Voltage level detectors: (a) block diagram of VLDs, (b) outputs of VLDs with different $V_{iSTH1,2}$.

In order to construct a VLD, two modified comparators are used. Fig. 6(a) shows several VLDs; V_{iSTH1} and V_{iSTH2} are variable lower and upper threshold voltages, respectively. Moreover, these $V_{iHET1,2}$ are adjustable as shown in Fig. 6(b) and 5(c). In Fig. 6(a), a master salve DFF removes unnecessary high frequency samples and a buffer isolates the VLD from the neural amplifier.

C. Digital demodulator (DD)

A DD comprises a RC circuit and a VLD (Fig. 7(a)). This DD can convert a burst of pulses to a single pulse. During a seizure, the VLD detects the abnormalities in signal and generates several bursts of pulses (V_{SDi}). Each of these pulses charges the capacitor (Ceb) quickly, but the discharging time of Ceb is longer than the duration between two consequent pulses of clock. Thus, the Ceb cannot be discharged completely during a burst of pulses. However, a VLD connected to RC circuit detects the end of the burst where the Ceb discharges completely through a diode connection of Meb1 transistor and generates a pulse (V_{Di}).

D. High frequency detector (HFD)

The HFD (Fig. 7(b)) has two main building blocks: the time frame selector (TFS) and the frequency detector (FD). The TFS consists of a RC circuit and a feedback (comparator with 0.5 V threshold voltage and DFF). The clock pulses charge the RC circuit and the feedback discharges the RC to zero. In Fig. 7(b), the V_{TF} controls the current flow through the RC circuit and Fig. 8(a) shows slopes of V_{CL} (Fig. 7(b)) for 7 kHz clock frequency (disconnecting the feedback) for various V_{TF}. Fig. 8(b) shows the corresponding charging time of the RC circuit (connecting the feedback) and Fig. 8(c)

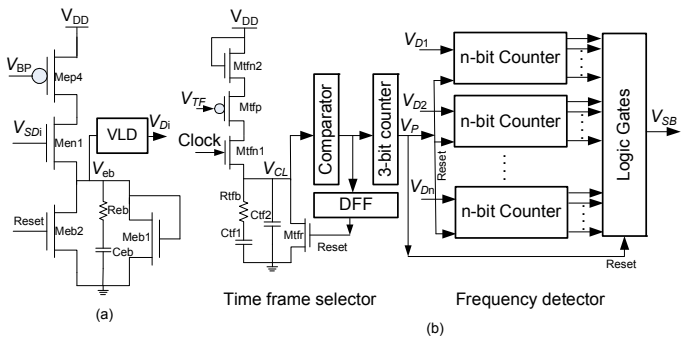

Fig.7. Schematic diagram of: (a) digital demodulator (b) high frequency detector.

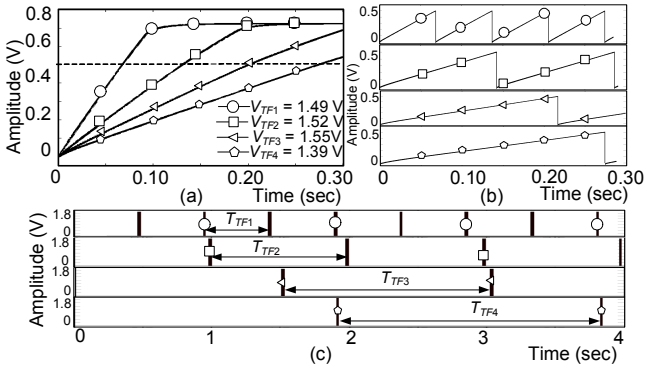

Fig. 8. Transient analysis of various time frame selection in Fig. 7(b): (a) different slopes of V_{CL} (without feedback), (b) V_{CL} with feedback, and (c) V_p defines duration of T_f.

shows outputs of 3-bit counter (V_p) (Fig. 8(b)) that defines duration of a time frame (T_f). On the other hand in Fig. 7(b), the FD counts number of pulses received from the DD (V_{Di}) and the V_p resets the FD at the end of every T_f. Finally, the logic gates declare the seizure detection (V_{SB}).

V. Simulation Results

A 30 year-old patient with intractable epilepsy underwent left craniotomy for invasive EEG evaluation. Two 10-contact subdural strip (F1 and F2) and a 64 contact subdural grid (G) electrodes were placed over the fronto-lateral, sub-frontal and fronto-temporal regions, respectively. Simulation was done using a segment or recording containing normal activity, a brief electrical seizure and an electroclinical seizure, as marked by an epileptologist (DKN) (Fig. 1). The signal from the contact showing earliest ictal changes during the seizures was fed into the SOD (Fig. 3) and fifteen seconds transient simulation results are shown in Fig. 9. The input signal (Fig. 9(a)) is modulated into 7 kHz sampling frequency (mid-frequency bandwidth of the preamplifier) and the input dynamic range of amplifier is adjusted to 10 µV to 100 µV (gain = 80dB). The amplified signal (V_{at}) (Fig. 10(b)) is passed through three VLDs to detect the specific features of the signal. From frequency and transient analysis of V_{at}, it is seen

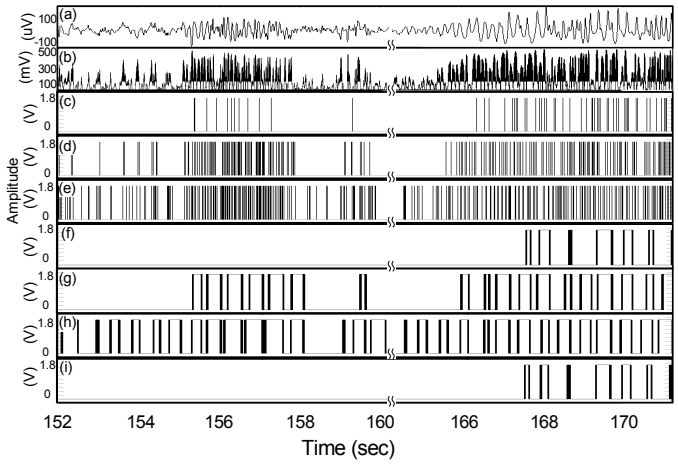

Fig. 9. Transient analysis of the detector: (a) seizure onset of Fig. 1,; (b) is modulated signal (V_{MOD}); (c)-(e) are outputs of VSDs (V_{SDi}); (f)-(h) are high frequency detection; and (i) is seizure onset detection.

TABLE I. Simulated Power Consumption (PC) (V_{DD} = 1.8V)

Block	PC (W)	Block	PC (W)
Preamplifier	6.70u	HFD[b]	6.30n
VLD[a]	387.18p	DD[c]	6.30n
Total power consumption			6.71u

[a]VLD: Voltage Level Detector, [b]HFD: High Frequency Detector, [c]DD: Digital Demodulator.

that the amplitude of the ictal pattern at onset for this patient is mainly between 100 mV and 450 mV. Thus, threshold voltages of the VLDs are set to 405 mV to 435 mV, 245 mV to 275 mV and 125 mV to 155 mV. Outputs of the VLDs (Fig. 9 (c)-(e)) are fed into a HFD to extract the frequency information. In the HFD, FD has three 3-bit counters and TFS determines T_f from the seizure frequency f_{STH} of the patient in Fig. 2(l) (T_f = 500 msec). The high frequency detections in the corresponding VLDs are shown in Fig. 9 (f)-(h). Finally, the SOD declares the seizure alert pulses (Fig. 9(i)) based on Fig. 9 (f)-(h). Table I summarizes the power consumed by the various functional blocks of the proposed detector.

VI. Conclusion

A low power (6.71uW) CMOS integrated low-voltage fast activity seizure onset detector has been demonstrated. The proposed detector provides the patient-specific tunable parameters to adjust to seizure onset patterns with the distinct amplitudes and frequencies. Several advantages of the proposed circuits were noted during the simulation. Moreover, the SOD exploits identification of progressive increases in amplitude of signal to eliminate false alarm due to biological source.

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