A Current-Mirror Opamp with Switchable Transconductances for Low-Power Switched-Capacitor Integrators

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***Abstract*- In a switched-capacitor (SC) integrator, the opamp can be switched off during the sampling phase, to reduce the power dissipation. This paper proposes a switchable-opamp technique based on a current-mirror opamp with switchable transconductances. Whereas previous switchable-opamp methods can only be used in SC integrators with half delay, the proposed technique can be utilized in SC integrators with both half delay, and full delay. Furthermore, no special common-mode feedback (CMFB) circuits are required for the opamp. At high sampling frequencies, circuit simulations of SC integrators and discrete-time ΔΣ modulators demonstrate that power reductions of 30% can be achieved by using the proposed technique, with minimal effect on the gain error of the SC integrator and the SNDR of the ΔΣ modulator. This confirms that the proposed switchable-opamp technique does not limit the speed of the SC circuit.**

I. Introduction

The switched-capacitor (SC) integrator is the basic building block of various SC filters, especially the loop filter of discrete-time (DT) ΔΣ modulators. Depending on the output sampling phase, a SC integrator can have either a *full delay* (Fig. 1a) or a *half delay* (Fig. 1b). During sampling phase ϕ_1, the integrator input is sampled on capacitor C_S (Fig. 2a), while the integrator output from the previous clock phase is held on feedback capacitor C_F. Since the integrator output does not change during ϕ_1, the opamp can be turned off during this sampling phase, in order to save power. During the charge-transfer phase ϕ_2, the charge sampled on C_S during the previous clock phase is transferred to C_F (Fig. 2b). Therefore the opamp must be fully operational during this charge-transfer phase.

Several switchable-opamp methods have been proposed to reduce the power dissipation in the integrators in SC filters and DT ΔΣ modulators. These include:

1. **Switched-Opamp (SO) method [1]**: Here, the integrator's opamp is fully switched off during the sampling phase (Fig. 3a). This can save up to 50% of the power consumption, compared to conventional designs with opamps fully active at all times [2]. However, this can limit the operation speed, due to the time required to turn on the opamps.
2. **Partially-Switched-Opamp (PSO) method [2,3]**: Here, a two-stage opamp is used and only its output stage is switched off during the sampling phase (Fig. 3b). By keeping the opamp's input stage on at all times, a faster turn-on time and, hence, operation speed can be achieved, compared to a SC integrator with an SO design. Furthermore, since the input stage may burn 1/4 of the opamp's total power consumption, power reductions of 40% can be typically achieved with a PSO design [2].

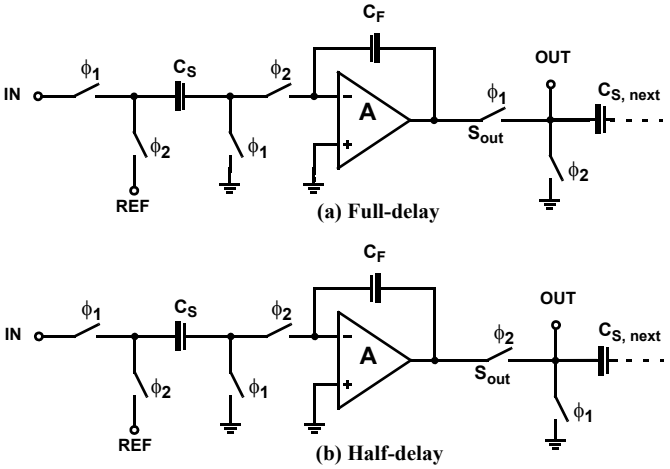

Fig. 1 A SC integrator with the loading effect of its next sampling stage capacitor $C_{S,\ next}$ shown: **(a)** a *full-delay* integrator; and **(b)** a *half-delay* integrator.

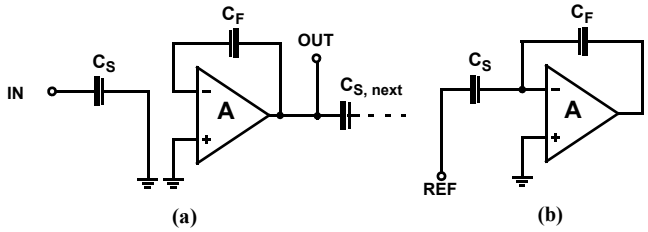

Fig. 2 A *full-delay* SC integrator during: **(a)** its sampling phase ϕ_1; and **(b)** its charge-transfer phase ϕ_2.

Another advantage of the SO and PSO methods is that the floating switch (S_{out} in Fig. 1b) can be eliminated, since the opamp output is in a high-impedance state during ϕ_2. This can improve the integrator linearity, especially in low-voltage designs. However, the associated disadvantage is that both the SO and PSO methods can only be employed in SC integrators with half delay, thereby restricting their use to specific DT ΔΣ modulator or SC filter architectures [4]. Furthermore, these opamps require special common-mode feedback (CMFB) circuits, since the opamp output is reset during the sampling phase [5].

This paper proposes a switchable-opamp for the low-power design of SC integrators. It is based on a current-mirror opamp architecture [6], but with transconductances that can be switched off during the sampling phase (Section II). It can be used in the design of SC integrators with both half-delay and

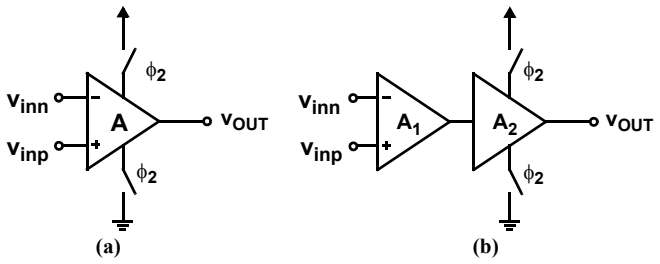

Fig. 3 Conceptual diagram of: **(a) the** switched-opamp; and **(b)** the partially-switched-opamp methods.

full-delay. Furthermore, since its input transconductance is on at all times, it doesn't suffer from operation-speed limitations found in SO designs. Simulation results confirm that power reductions of up to 30% can be achieved in SC integrators by using the proposed switchable-opamp (Section IV), compared to having the current-mirror opamp fully active at all times.

Section II illustrates the proposed switchable-opamp technique. Section III then describes its circuit realization. Section IV presents circuit simulation results to confirm the functionality and the performance advantages of the proposed technique in SC integrators and DT ΔΣ modulators.

II. Proposed Switchable-Opamp

Consider the proposed opamp, whose conceptual diagram is shown in Fig. 4, where:

- *Gm* = input transconductance
- *K* = current-mirror gain
- *KGm* = total output transconductance
- α = transconductance switching ratio

The total output transconductance and its load are split into two parts with the ratio α. The α part of the total transconductance and its load is switched off during the sampling clock phase ϕ_1, while the (1- α) part remains on at all times. Accordingly, the proposed opamp in Fig. 4 has the following advantages:

1. Since the opamp output is available during both clock phases, this opamp can be used to realize both full-delay (Fig. 1a), and half-delay (Fig. 1b) SC integrators. Furthermore, classical SC CMFB circuits can be used with this opamp.
2. During the charge-transfer clock phase ϕ_2, the opamp is operated at its full output transconductance (*K Gm)*, in order to maximize the unity-gain bandwidth ω_t and, hence, achieve the targeted settling accuracy. However, the opamp does not need a high ω_t during the sampling clock phase ϕ_1, as its output does not change during ϕ_1. Therefore, by turning off part of the opamp's output transconductance during ϕ_1, power savings can be achieved.
3. Since the opamp's input transconductance and part of its output transconductance are on at all times, this opamp doesn't suffer from the operation speed limitations found in SO designs.

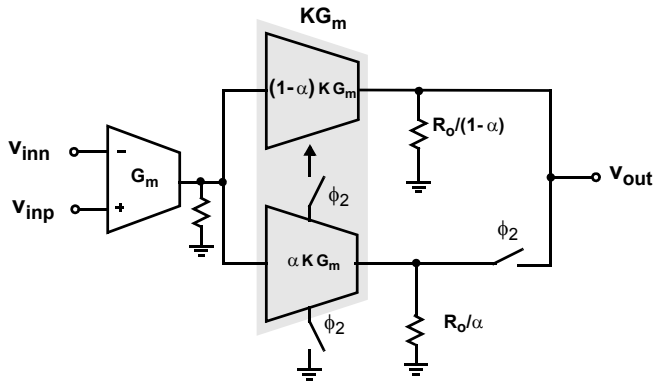

Fig. 4 Conceptual diagram of the proposed switchable-opamp.

III. Design of The Proposed Switchable-Opamp

A. Circuit implementation

Consider a classical current-mirror opamp (the circuit in Fig. 5 with α = 0) having a current gain (from input to output) of *K* [6]. At a given total bias current (power dissipation), if the unity-gain frequency is limited by the load capacitance, increasing *K* increases both the unity-gain bandwidth and the slew-rate, at the expense of an increase in phase margin and in the input-referred thermal noise. A practical limit on *K* might be around 5 [6].

To realize the switchable opamp in Fig. 4, the output transistors of the current-mirror opamp in Fig. 5 are split with a ratio of α to (1- α). The α part is switched on during ϕ_2 only. Transistor-fingering layout techniques enable realizing various values of α.

B. Power Saving

The supply current in a classical current-mirror opamp (the circuit in Fig. 5 with α = 0) is

$$I_{DD,avg}\big|_{classical} = 2I_B + 2KI_B \qquad (1)$$

where $2I_B$ is the input differential-pair bias current (Fig. 5). Assuming a clock duty cycle of 50%, the supply current (averaged over a clock period) in the proposed opamp (Fig. 5) is

$$I_{DD,avg}\big|_{proposed} = 2I_B + (2-\alpha)KI_B \qquad (2)$$

Therefore, the reduction in supply current, achieved by the proposed switchable-opamp technique, is

$$\Delta I_{DD,avg} \equiv I_{DD,avg}\big|_{classical} - I_{DD,avg}\big|_{proposed} = \alpha KI_B \qquad (3)$$

This results in a power-dissipation saving of

$$\frac{\Delta I_{DD,avg}}{I_{DD,avg}\big|_{classical}} = \frac{\alpha/2}{1+1/K} \qquad (4)$$

Figure 6 plots the relative power-dissipation saving in (4) versus the switching ratio α, for various current gains *K*.

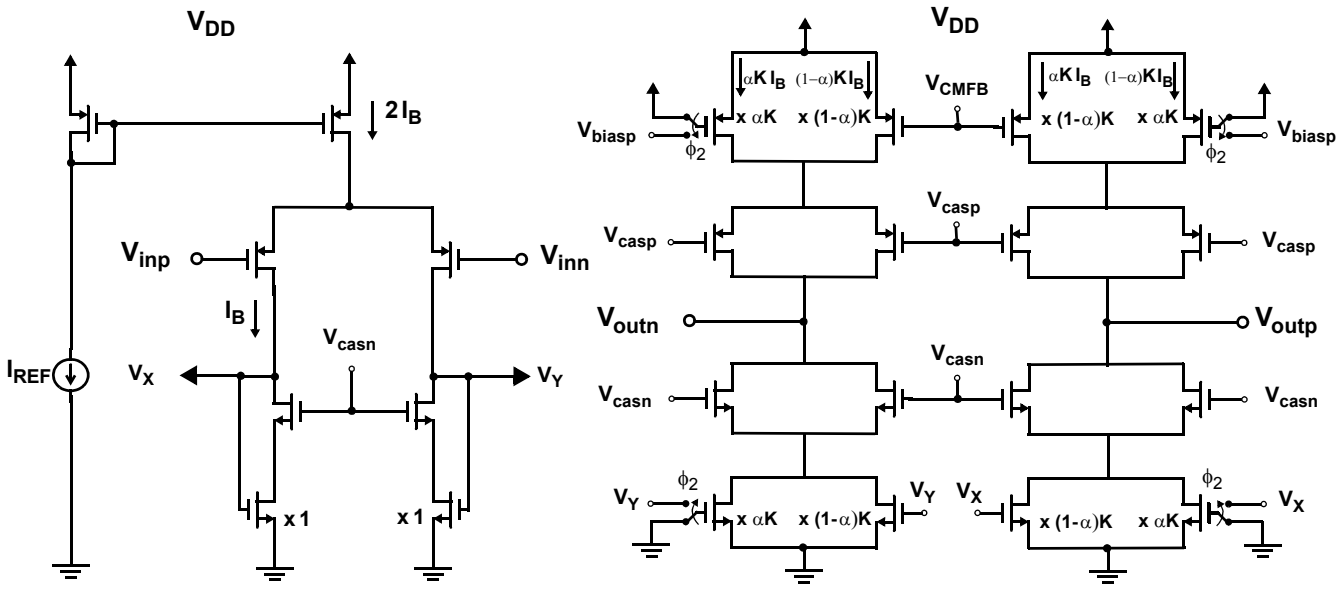

Fig. 5 Circuit diagram of the proposed switchable-opamp.

IV. Circuit Simulation Results

The proposed switchable-opamp circuit (Fig. 5) was designed in a 1-V 65-nm CMOS process, with a current gain of $K = 4$, to achieve the following specifications when $\alpha = 0$ (i.e. for a classical current-mirror opamp configuration):

- DC gain of $A_0 = 165$ V/V.
- Unity-gain bandwidth of $f_T = 725$ MHz (at a 1.5-pF load).
- Phase-margin of $PM = 80^o$ (at a feedback factor of 0.5).

The above opamp was used to realize a full-delay SC integrator (Fig. 1a) with:

- Sampling frequency of $f_S = 128$MHz.
- Sampling capacitor of $C_S = 1.5$pF.
- Integrator gain of $K_I = C_S/C_F = 1$.
- Next-stage sampling capacitor of $C_{S,\,next} = 0.5$pF.

The SC integrator was then simulated, in order to demonstrate how using the proposed switchable opamp can impact the performance of a SC integrator.

A. Gain error of the SC integrator

When a step voltage of height $V_{in,\,step}$ is applied at the input of an ideal SC integrator, the resulting change at the output is $K_I V_{in,\,step}$, where $K_I = C_S/C_F$ is the integrator gain. Therefore, the gain error of the SC integrator can be expressed as [7]:

$$\varepsilon \equiv \frac{\left|K_I V_{in,\,step}\right| - \left|V_{out,\,sampled}\right|}{\left|K_I V_{in,\,step}\right|} = \varepsilon_g + \varepsilon_{sett} \qquad (5)$$

where $V_{out,sampled}$ is the integrator's output sampled at the end of ϕ_1, ε_g is the integrator's gain error due to the opamp's finite dc gain, and ε_{sett} is the integrator's gain error due to opamp dynamics (finite bandwidth and slew rate) [7]. For the SC integrator specified above, $\varepsilon_g = 0.015$ and $\varepsilon_{sett} = e^{-5}$ with no switching ($\alpha = 0$).

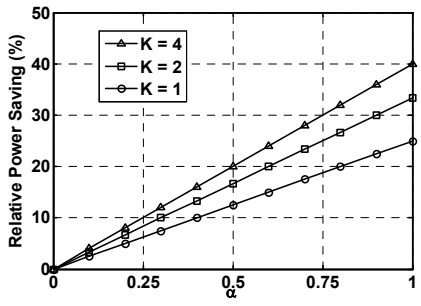

Fig. 6 Relative power-dissipation saving, achieved using the proposed switchable opamp (Fig. 5) vs. switching ratio α, for various current gains K.

Table I reports the gain error ε of the SC integrator and the achievable power savings using the proposed switchable-opamp for various settings of the opamp's switching ratio α, for a small and a large input step. Observe that ε remains approximately constant until α reaches 0.75. It then increases by about 8% for a small input step (20% for a large input step). Accordingly, while there is a power accuracy trade-off in the choice of α (primarily due to the increase in the time required for the opamp to switch back to its full operation state as α increases), an $\alpha = 0.75$ results in about 30% reductions in power dissipation without significantly affecting the integrator's gain error (especially, for small input steps).

TABLE I. SC integrator's gain error ε and the achievable power savings using the proposed switchable opamp for various settings of the opamp switching ratio α, at a 50-mV and 250-mV input steps.

α	Gain error ε (%)		$I_{DD,\,avg}$ (mA)	Power saving (%)
	50-mV step input	250-mV step input		
0 (no switching)	2.2	2.5	1.35	0
0.25	2.2	2.5	1.21	10.3
0.5	2.2	2.5	1.09	19.2
0.75	2.4	3	0.96	28.8

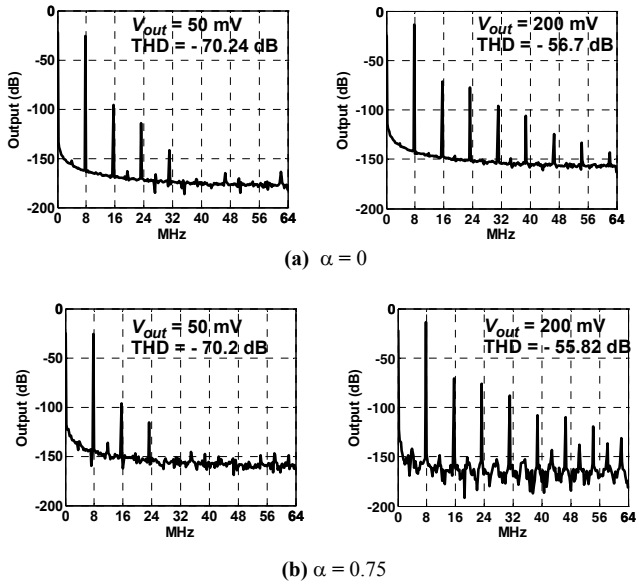

Fig. 7 Output Spectrum of the SC integrator with a 20-mV, and an 80-mV input sinusoid, resulting in an output sinusoid having V_{out} = 50 mV and V_{out} = 200mV. Two cases are considered for the switching ratio of the integrator's opamp: **(a)** α = 0 (No switching); and **(b)** α = 0.75.

B. Linearity of the SC integrator

A 7.75-MHz sinusoid with amplitudes of V_{in} = 20 and 80mV is applied at the input of the SC integrator, resulting in a sinusoid at the output with amplitudes of V_{out} = 50 and 200mV. A threshold-voltage mismatch of ±3 mV is added between the switching transistors on the positive and negative output sides of the opamp. Figure 7 shows the integrator's output spectrum when V_{in} = 20mV (V_{out} = 50mV) and V_{in} = 80mV (V_{out} = 200mV), when: a) α = 0; and b) α = 0.75. The difference in total harmonic distortion (THD) between the two cases (α = 0 and α = 0.75) is less than 1 dB, at both output levels (V_{out} = 50mV and 200mV).

C. Performance of the DT ΔΣ modulator

The second-order 3-bit ΔΣ modulator with analog feedforward in Fig. 8 [8] is simulated for an OSR of 32. The proposed switchable-opamp technique is used in both integrators.

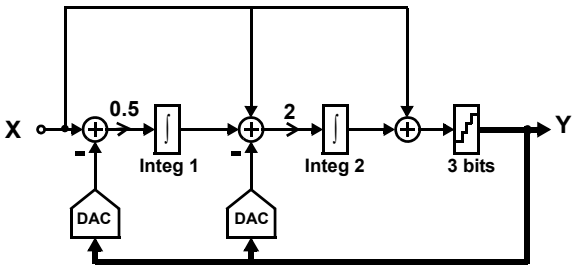

Fig. 8 The simulated second-order ΔΣ modulator.

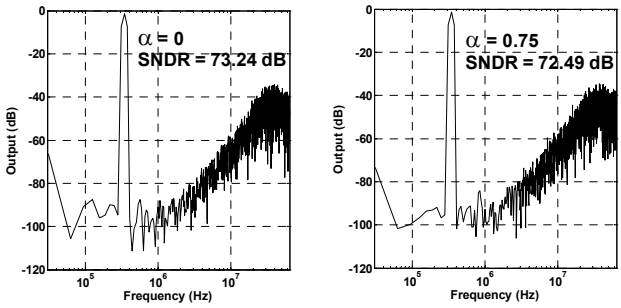

Fig. 9 Output Spectrum of the ΔΣ modulator in Fig. 8, when the opamps of its integrators have a switching ratio of: **(a)** α = 0 (no switching); and **(b)** α = 0.75.

Figure 9 shows the output spectrum of the ΔΣ modulator for a -1.4 dBFS input, when opamps with α = 0 and α = 0.75 are used. The difference in SNDR between the two cases (due the incomplete-settling errors) is less than 1 dB, while a reduction of around 28.6% in the power dissipation of each integrator is achieved when α = 0.75.

V. CONCLUSION

A switchable-opamp technique is proposed for the low-power design of SC integrators. Compared to previous opamp-switching methods, the proposed technique is applicable to SC integrators with both full delay and half delay. Furthermore, it does not limit the operation speed of the SC integrator and does not require a special CMFB circuit.

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