Digital Background Calibration of Capacitor-Mismatch Errors in Pipelined ADCs

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***Abstract*—A digital background calibration technique is proposed to correct for the linearity error due to capacitor mismatches in pipelined analog-to-digital converters (ADCs). During the normal ADC operation, it randomly swaps the feedback capacitor with the sampling capacitor(s) in the multiplying digital-to-analog converter (MDAC) of each pipeline stage in the pipelined ADC. The capacitor-mismatch errors in all pipeline stages are then concurrently measured and corrected in the digital domain. The proposed technique can be utilized in both single-bit and multibit MDACs. Owing to its simple iterative algorithm for capacitor-mismatch error calibration, its implementation requires minimal additional digital hardware. Behavioral simulation results show that, using the proposed calibration technique, the signal-to-noise-plus-distortion ratio is improved from 10 to 12.5 bits and the spurious-free dynamic range is increased from 65 to 95 dB, in a 13-bit pipelined ADC with $\sigma = 0.25\%$ capacitor mismatches.**

***Index Terms*—Analog-to-digital conversion, capacitor mismatch, digital background calibration, pipelined analog-to-digital converter (ADC).**

I. Introduction

THE linearity of a pipelined analog-to-digital converter (ADC) is primarily degraded by the linearity errors in its pipeline stages. Consider a typical pipeline stage with digital redundancy [1], as depicted in Fig. 1. In a switched-capacitor circuit implementation, the primary sources of linearity errors are: 1) the gain errors in the residue amplifier, due to the finite gain and dynamic effects of its operational amplifier [2]; and 2) the nonlinearity in the digital-to-analog subconverter (sub-DAC), due to capacitor-mismatch errors. Compared to gain errors, capacitor-mismatch errors have a significantly more degrading effect on the overall linearity of the pipeline stage [1], [3].

This brief proposes a digital background calibration technique to measure and correct for capacitor-mismatch errors in the pipeline stages of a pipelined ADC. The proposed technique randomly swaps the feedback capacitor with the sampling capacitor(s) in the multiplying DAC (MDAC) of each pipeline stage. Both the measurement and calibration of the capacitor-mismatch errors in each pipeline stage are then performed entirely digitally, using simple logic circuits. Thus, no additional high-precision analog circuits are required [4]. Furthermore, the measurement and calibration of the capacitor-mismatch errors in all pipeline stages are performed concurrently during the normal ADC operation, without requiring any special calibration signal [5] to be injected at the input of the pipeline stages.

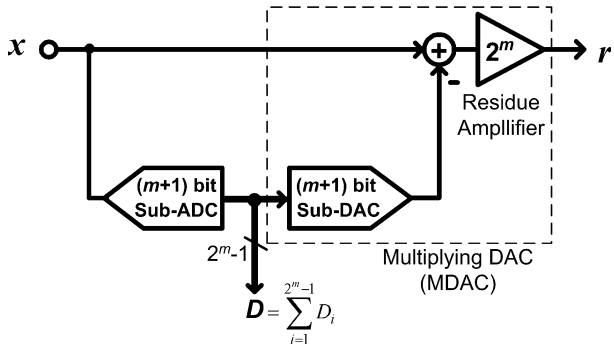

Fig. 1. Pipeline stage with an m-bit effective resolution and a 1-bit redundancy for digital error correction.

Other digital background calibration techniques, which utilize capacitor shuffling or capacitor swapping to mitigate the linearity error due to capacitor mismatches in pipelined ADCs, have been suggested in [3], [6]–[8]. However, the calibration technique in [3] targets multibit pipeline stages only (with large digital circuits required to implement its capacitor-shuffling logic [9]), while the calibration technique in [6] is only intended for single-bit pipeline stages. In [7], a DAC-and-feedback capacitor averaging (DFAC) technique spreads the signal harmonics, followed by a hardware-intensive mismatch noise cancellation (MNC) technique [8]. Hence, when using the DFCA technique, the spurious-free dynamic range (SFDR) of the ADC is improved, but not its signal-to-noise-and-distortion ratio (SNDR), because its noise floor is not decreased.

In this brief, the proposed digital background-calibration technique uses a simple iterative algorithm for capacitor calibration (Section II) and, hence, it can be implemented using simple digital logic. Furthermore, it significantly improves both the SFDR and SNDR in single-bit and multibit pipeline stages, as confirmed by the behavioral simulation results (Section III).

Throughout this brief, the capacitor-mismatch errors are assumed to be the dominant contributors to the overall linearity error of the pipelined ADC, as is typically the case [1], [3]. The gain errors are assumed to be corrected for using a gain-calibration method, such as in [10]–[12]. In the proposed capacitor-calibration technique, gain errors have a negligible effect on correcting for the capacitor-mismatch errors (Section II).

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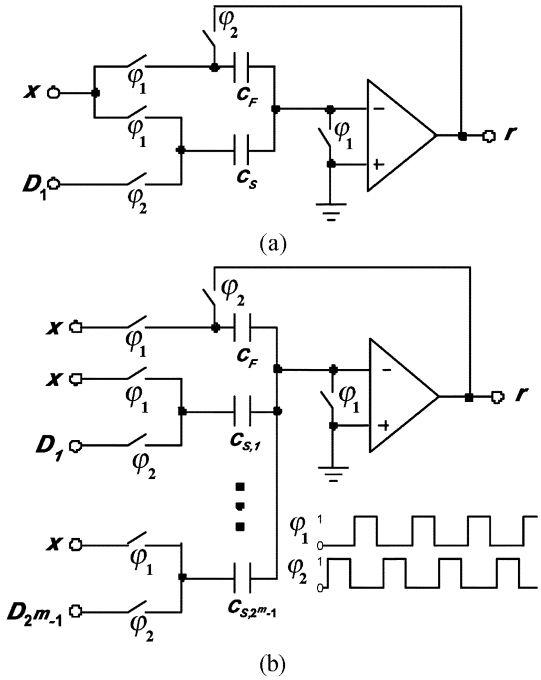

Fig. 2. Capacitor flip-over MDAC for: (a) 1-bit or 1.5-bit pipeline stages; and (b) m-bit pipeline stages (Fig. 1).

II. Proposed Calibration Technique

A. Digital Calibration of 1-bit Pipeline Stages

Consider the "capacitor-flip-over" MDAC in Fig. 2(a), which is widely utilized to realize 1-bit pipeline stages. Define the capacitor-mismatch error as

$$\delta C \equiv (C_S - C_F)/C_F \tag{1}$$

where C_S and C_F are the sampling and feedback capacitors, respectively. Then, the MDAC residue (output) signal is

$$r = \left(2x\left(1+\frac{\delta C}{2}\right) - D_1(1+\delta C)V_{\text{ref}}\right)(1+\delta g) \tag{2}$$

where δg represents the gain error due to opamp nonidealities. Here, digit D_1 (i.e., the sub-ADC output in Fig. 1) is either $+V_{\text{ref}}$ or $-V_{\text{ref}}$, depending on input signal x. A unity reference voltage ($V_{\text{ref}} = 1$) will be assumed for simplicity.

In the following, the gain error δg is assumed to be corrected for by a gain-calibration method [10]–[12] and, hence, a zero gain error ($\delta g = 0$) can be assumed. The effect of δg on correcting for δC is discussed in the next subsection.

In the proposed calibration technique, the roles of capacitors C_S and C_F are randomly interchanged (i.e., C_S and C_F are randomly swapped) during the hold clock-phase φ_2 in order to digitally measure the capacitor-mismatch error δC. As depicted in Fig. 3, such capacitor swapping is achieved using a pseudorandom control signal N with a value of $+1$ (to connect C_F in feedback) or -1 (to connect C_S in feedback). Thus, when $N = -1$, the roles of C_F and C_S are interchanged, and, hence, the value of δC must be interchanged with

$$\delta C|_{N=-1} = \frac{C_F - C_S}{C_S} = -(\delta C + \delta C^2) \approx -\delta C \tag{3}$$

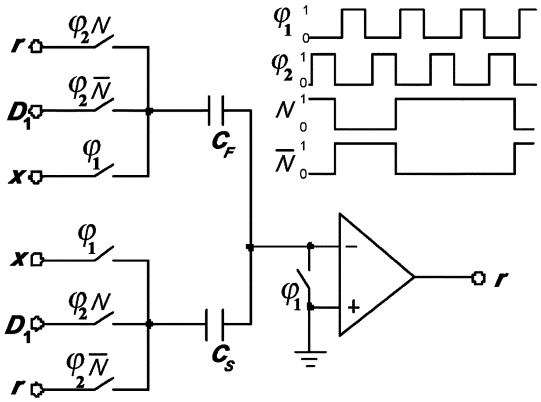

Fig. 3. The 1-bit MDAC in Fig. 2(a) with capacitors C_S and C_F randomly swapped, using a pseudorandom control signal N in order to digitally measure the capacitor-mismatch error δC. Note that the values $N = 0, 1$ depicted in the figure correspond to the values $N = -1, 1$ used in the text.

in (2). Accordingly, the MDAC residue signal r can be expressed for both values of N as

$$r = 2x\left(1 + N\frac{\delta C}{2}\right) - D_1(1 + N\,\delta C). \tag{4}$$

Let R denote the digital representation of the MDAC residue signal r in (4). Assume that the value of r is digitized (by the subsequent pipeline stages in the pipelined ADC) as R, without any error. Then, using (4), the corrected value of R is

$$\widehat{R} = 2x\left(1 + N\frac{(\delta C - \widehat{\delta C})}{2}\right) - D_1\left(1 + N\,(\delta C - \widehat{\delta C})\right) \tag{5}$$

where $\widehat{\delta C}$ denotes the estimated value of δC.

To estimate the value of capacitor-mismatch error δC, assume that the pseudorandom control signal N has a zero mean value (i.e., both C_F and C_S are equally utilized as the feedback capacitor). Then, since $N^2 = 1$ and $D_1^2 = 1$ (for a 1-bit MDAC), defining

$$V_{\widehat{RND}} \equiv \widehat{R} - N\,D_1 \tag{6}$$

results in

$$V_{\widehat{RND}} = (xD_1 - 1)(\delta C - \widehat{\delta C}) + (2xD_1 - 1)N. \tag{7}$$

If the estimated value $\widehat{\delta C}$ is equal to the actual value δC, then the average value of $V_{\widehat{RND}}$ will be zero (since N and x are independent and N has a zero mean value). Therefore, by starting with an initial value for $\widehat{\delta C}$ and then utilizing $V_{\widehat{RND}}$ to iteratively update $\widehat{\delta C}$ in the digital domain, the estimated value $\widehat{\delta C}$ will converge to the actual value δC. Accordingly, $\widehat{\delta C}$ can be iteratively updated in the digital domain using

$$\widehat{\delta C}\,(n+1) = \widehat{\delta C}\,(n) - \varepsilon V_{\widehat{RND}} \tag{8}$$

where n is the iteration index and ε is the update step size. Note that the factor $(xD_1 - 1)$ in (7) is always negative (as, ideally, $|x| < 1$ and $D_1 = \text{sign}(x)$). Hence, the average value of $V_{\widehat{RND}}$

is positive/negative when $\widehat{\delta C}$ is larger/smaller than δC. Thus, the negative sign in (8) ensures that $\widehat{\delta C}$ converges to δC. Further, by decreasing the value of ε, the effect of input-signal interference in estimating δC is suppressed. However, for a given resolution, this increases the time required to estimate δC [11].

B. Digital Calibration of 1.5-bit Pipeline Stages

The MDAC in Fig. 2(a) is also widely utilized to realize 1.5-bit pipeline stages. In this case, digit D_1 is ± 1 or 0, depending on input signal x. When $D_1 = 0, V_{\widehat{RND}} = 0$ and, hence, iterative relation (8) is not affected. Therefore, the proposed calibration technique described above for 1-bit pipeline stages (where $D_1 = \pm 1$) can be directly utilized in 1.5-bit pipeline stages (where $D_1 = \pm 1$ or 0), as confirmed by the simulation results in Section III.

It is important to point out the following characteristics of the proposed capacitor-mismatch calibration technique.

1) **Effect of gain error on capacitor-mismatch calibration:** For a nonzero gain error δg in (2), (5) must be rewritten as

$$\widehat{R} = 2x\left(1 + N\frac{((1+\delta g)\delta C - \widehat{\delta C})}{2}\right) - D_1(1 + N((1+\delta g)\delta C - \widehat{\delta C})). \quad (9)$$

Comparing (5) and (9) reveals that, in the proposed calibration technique, the estimated value $\widehat{\delta C}$ for the capacitor-mismatch error δC converges to

$$\widehat{\delta C} = (1+\delta g)\delta C. \quad (10)$$

Thus, if $\delta g \neq 0$, the error in estimating δC is $\delta g \cdot \delta C$. This error is negligibly small, as δg has a small value. Accordingly, in the proposed calibration technique, the gain error δg has a negligible effect on estimating the capacitor-mismatch error δC.

2) **Fully differential MDAC:** The differential residue signal of a fully differential MDAC can be expressed as

$$r_{\text{diff}} = 2x\left(1 + \frac{\delta C_p + \delta C_n}{2}\right) - D_1(1 + \delta C_p + \delta C_n)V_{\text{ref}} \quad (11)$$

where δC_p and δC_n are the mismatch errors between the sampling and feedback capacitors in the *positive* and *negative* paths of the fully differential MDAC, respectively. When performing the proposed capacitor swapping, r_{diff} in (11) can be expressed for both values of N as

$$r_{\text{diff}} = 2x\left(1 + N\frac{\delta C_p + \delta C_n}{2}\right) - D_1(1 + N(\delta C_p + \delta C_n))V_{\text{ref}}. \quad (12)$$

Comparing (4) and (12) reveals that, by considering the single-ended mismatch error δC in (4) to be the differential mismatch error $(\delta C_p + \delta C_n)$, iterative relation (8) can be utilized in a fully differential MDAC to digitally estimate its capacitor-mismatch error $(\delta C_p + \delta C_n)$. Thus, the proposed calibration technique is also applicable to fully differential MDACs.

3) **Input signal:** Iterative relation in (8) assumes no specific input signal x for the pipeline stage (Fig. 1), except for the corresponding most significant digit D_1 at the sub-ADC output being nonzero. With no redundancy bits, D_1 is always nonzero. With m effective bits and 1-bit redundancy, D_1 is zero for input signals between $\pm V_{\text{ref}}/2^{m+1}$. Hence, the proposed calibration technique is applicable for any input signal (including dc), except for input signals limited between $\pm V_{\text{ref}}/2^{m+1}$ in m-bit pipeline stages with 1-bit redundancy.

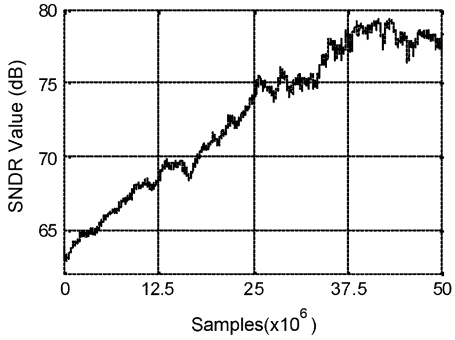

Fig. 4. SNDR values during the normal operation of the pipelined ADC.

C. Digital Calibration of Multibit Pipeline Stages

Consider the multibit MDAC in Fig. 2(b), which is used to realize pipeline stages with an m-bit effective resolution (Fig. 1). Define the mismatch error in each sampling capacitor as

$$\delta C_k \equiv (C_{S,k} - C_F)/C_F, \qquad k = 1, \ldots, 2^m - 1 \quad (13)$$

where C_F is the feedback capacitor and $C_{S,k}$ $(k = 1, \ldots, 2^m - 1)$ are the sampling capacitors. Then, the MDAC residue (output) signal r can be expressed as

$$r = 2^m x\left(1 + \frac{1}{2^m}\sum_{i=1}^{2^m-1}\delta C_i\right) - \sum_{i=1}^{2^m-1} D_i(1+\delta C_i)V_{\text{ref}}. \quad (14)$$

Here, each digit D_i is 0 or ± 1, based on input signal x.

In the proposed calibration technique, a capacitor-shuffling digital logic is utilized in an m-bit MDAC [see Fig. 2(b)] to perform the following tasks during the hold clock phase φ_2.

1) Select a sampling capacitor $C_{S,M}$ for calibration, based on a random selection signal $M (M = 1, \ldots, 2^m - 1)$.
2) Connect $C_{S,1}$ to either $\pm V_{\text{ref}}$ or 0, based on D_M.
   Connect $C_{S,M}$ to either $\pm V_{\text{ref}}$ or 0, based on D_1.
   Here, D_1 is the most significant digit of the sub-ADC output in the multibit pipeline stage (Fig. 1) and, hence, is predominantly $+1$ or -1. Thus, connecting capacitor $C_{S,M}$ to D_1 (rather than D_M) ensures that the digit connected to the capacitor under calibration is predominantly nonzero.
3) Swap $C_{S,M}$ with C_F, based on random control signal N.
   If $N = +1$, connect C_F to signal r and connect $C_{S,M}$ to $\pm V_{\text{ref}}$ or 0, based on D_1.

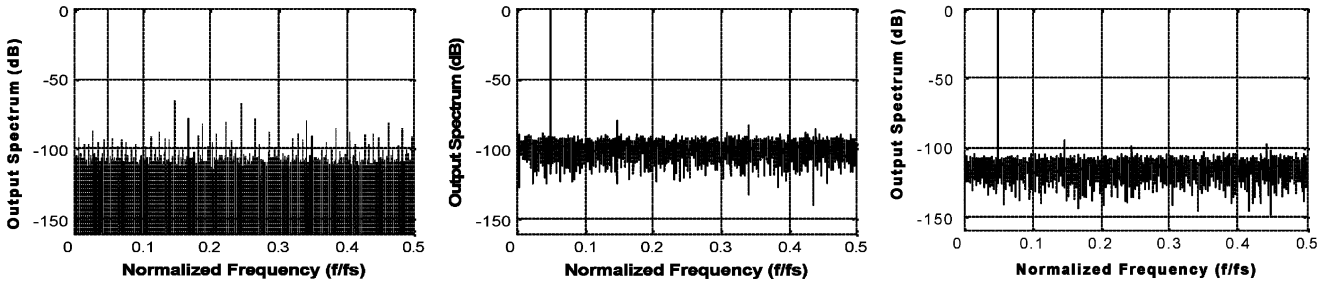

Fig. 5. Output spectrum of the pipelined-ADC when: (a) capacitor swapping is OFF and capacitor calibration is OFF, (b) capacitor swapping is ON and capacitor calibration is OFF, and (c) capacitor swapping is ON and calibration is ON.

If $N=-1$, connect $C_{S,M}$ to signal r and C_F to $\pm V_{\text{ref}}$ or 0, based on D_M.

Similar to the 1-bit MDAC case, swapping $C_{S,M}$ and C_F in an m-bit MDAC (as described above) permits estimating capacitor-mismatch errors δC_M in the digital domain using the iterative relation (Appendix A)

$$\widehat{\delta C}_M\,(n+1)=\widehat{\delta C}_M\,(n)-\varepsilon V_{\widehat{RND}}, \qquad M=1,\ldots,2^m-1 \tag{15}$$

$$V_{\widehat{RND}}=\widehat{R}\;N\,D_1 \tag{16}$$

where n is the iteration index and ε is the update step size. Here, $\widehat{\delta C}_M$ is the estimated value of δC_M. Defining R as the digital representation of the MDAC residue signal r in (14), then $\widehat{R}$ is the corrected value of R, after calibration using the estimated values $\widehat{\delta C}_M$ for capacitor-mismatch errors δC_M.

In the m-bit MDAC of Fig. 2, the number of switches is $4\times 2^m-1$. To implement the proposed capacitor shuffling (described above), the number of extra switches needed is only 2^m+2, with 2^m-1 extra switches connecting each $C_{S,M}$ to residue signal r and three extra switches connecting C_F to the 3-level $(-V_{\text{ref}},0,+V_{\text{ref}})$ digit D_1. Such switch overhead compares favorably with other previously reported calibration methods based on capacitor shuffling [3], [6]–[8].

III. Simulation Results

The proposed calibration technique is implemented in a 13-bit pipelined ADC. The pipeline core of this ADC is partitioned into a 2.5-bit first stage, followed by eleven 1.5-bit stages. Behavioral simulations of this ADC are performed in SIMULINK, assuming random capacitor-mismatch errors (δC) of 0.25% (1σ) in each pipeline stage. Only the first, second, and third pipeline stages of the ADC are calibrated, as its overall performance is most sensitive to the nonidealities in its front-end stages. The calibration of the capacitor-mismatch errors in all pipeline stages is performed concurrently during the normal ADC operation. Uncorrelated random control signals (N) are utilized for each pipeline-stage calibration. In the iterative relations for capacitor-mismatch estimation in (8) and (15), the update step size ε is set to 2^{-22}. A full-scale sine wave signal is applied at the ADC input.

Fig. 4 shows the converter SNDR during the initial convergence of the calibration algorithm, while the ADC is in normal operation. Accordingly, to achieve SNDR values greater than 12 bits (74 dB), the required number of samples is approximately 30×10^6 samples. Such number of convergence samples compares favorably with that required to achieve a 12-bit resolution using previously proposed calibration techniques [3], [5].

TABLE I
Summary of Behavioral Simulation Results

Swapping / Calibration	SNDR	SFDR
OFF / OFF	62 dB	65 dB
ON / OFF	61.5 dB	79.5 dB
ON / ON	77 dB	95 dB

Fig. 5 shows the output spectrum of the pipelined ADC when performing: 1) no capacitor swapping and no capacitor-error calibration; 2) only capacitor swapping; or 3) both capacitor swapping and capacitor-error calibration. The corresponding SNDR and SFDR of the ADC are summarized in Table I. Accordingly, capacitor swapping by itself only spreads the signal harmonics and, therefore, only improves the SFDR (as in [7]). With both capacitor swapping and capacitor-error calibration, the proposed calibration technique achieves approximately a 12.5-bit SNDR and a 95-dB SFDR for a 13-bit pipelined ADC.

IV. Conclusion

A digital background calibration technique was proposed to correct for capacitor-mismatch errors in pipelined ADCs. It is applicable to both 1.5-bit and multibit pipeline stages. Behavioral simulation results confirmed its effectiveness in significantly improving both the resolution and linearity of pipelined ADCs, even in the presence of large capacitor-mismatch errors. Since the proposed technique utilizes relatively simple relations to estimate the capacitor-mismatch errors, only a small digital circuit block should be needed to implement its calibration logic.

Appendix

In this Appendix, expression (15) for estimating the capacitor-mismatch error in a multibit MDAC is derived. Specifically, consider the m-bit MDAC in Fig. 2(b). Assume that the sampling capacitor $C_{S,1}$ is under calibration. Then, to measure the mismatch error δC_1, the roles of capacitors $C_{S,1}$ and C_F are randomly interchanged during the hold clock phase φ_2. Such capacitor swapping is controlled by a pseudorandom control signal N with a value of ± 1. When $N=1, C_F$ is the feedback capacitor and the MDAC residue signal r is expressed as in (14), with the capacitor-mismatch errors δC_k expressed as

in (13). When $N = -1$, the roles of $C_{S,1}$ and C_F are interchanged. Therefore, the values for the MDAC residue signal r must be interchanged with

$$\delta C_k|_{N=-1} = \frac{C_F - C_{S,1}}{C_{S,1}} = -\left(\delta C_1 + \delta C_1^2\right) \approx -\delta C_1, \quad \text{for } k = 1 \tag{17}$$

$$\delta C_k|_{N=-1} = \frac{C_{S,k} - C_{S,1}}{C_{S,1}} = (\delta C_k - \delta C_1)\frac{C_F}{C_{S,1}} \approx \delta C_k - \delta C_1, \quad \text{for } k = 2, \ldots, 2^m - 1. \tag{18}$$

Accordingly, the MDAC residue signal can be expressed for both values of N as

$$\begin{aligned} r = &\left(1 + \frac{N\delta C_1}{2^m} + \frac{1}{2^m}\sum_{i=2}^{2^m-1}\left(\delta C_i - \frac{(1-N)}{2}\delta C_1\right)\right)2^m x \\ &- (1 + N\delta C_1)D_1 - \sum_{i=2}^{2^m-1} D_i \\ &\times \left(1 + \left(\delta C_i - \frac{(1-N)}{2}\delta C_1\right)\right). \end{aligned} \tag{19}$$

Let R denote the digital representation of the MDAC residue signal r in (19). Assume that the value of r is digitized (by the subsequent pipeline stages in the ADC) as R, without any error. Then, using (19), the corrected value of R is

$$\begin{aligned} \widehat{R} = &\left(1 + \frac{N(\delta C_1 - \widehat{\delta C_1})}{2^m} + \frac{1}{2^m}\sum_{i=2}^{2^m-1}\left(\delta C_i - \frac{(1-N)}{2}(\delta C_1 - \widehat{\delta C_1})\right)\right)2^m x \\ &- (1 + N(\delta C_1 - \widehat{\delta C_1}))D_1 \\ &- \sum_{i=2}^{2^m-1} D_i\left(1 + \delta C_i - \frac{(1-N)}{2}(\delta C_1 - \widehat{\delta C_1})\right) \end{aligned} \tag{20}$$

where $\widehat{\delta C_1}$ denotes the estimated value of capacitor-mismatch error δC_1. TAssume that the pseudorandom control signal N has a zero mean value. Then, since $N^2 = 1$

$$V_{\widehat{RND}} \equiv \widehat{R}\ N\ D_1 \tag{21}$$

results in

$$V_{\widehat{RN}\ D} = k_1(\delta C_1 - \widehat{\delta C_1}) + k_2\ N \tag{22}$$

where

$$k_1 = \left(1 + \sum_{i=2}^{2^m-1}\frac{1}{2}\right)D_1\ x - D_1^2 - \left(\sum_{i=2}^{2^m-1}\frac{D_i}{2}\right)D_1 \tag{23}$$

$$k_2 = \left(2^m + \sum_{i=2}^{2^m-1}\delta C_i - \frac{(\delta C_1 - \widehat{\delta C_1})}{2}\right)D_1\ x - D_1^2 - \left(\sum_{i=2}^{2^m-1} D_i\left(1 + \delta C_i - \frac{(\delta C_1 - \widehat{\delta C_1})}{2}\right)\right)D_1. \tag{24}$$

Thus, the average value of $V_{\widehat{RND}}$ is proportional to $(\delta C_1 - \widehat{\delta C_1})$, as N and x are independent and N has a zero mean value. Therefore, by starting with an initial value for $\widehat{\delta C_1}$ and then utilizing $V_{\widehat{RND}}$ to iteratively update $\widehat{\delta C_1}$ in the digital domain, the estimated value $\widehat{\delta C_1}$ will converge to the actual value δC_1. Accordingly, $\widehat{\delta C_1}$ can be iteratively updated using

$$\widehat{\delta C_1}\ (n+1) = \widehat{\delta C_1}\ (n) - \varepsilon V_{\widehat{RND}} \tag{25}$$

where n is the iteration index and ε is the update step size.

To estimate each of the other capacitor-mismatch errors $\delta C_k (k = 2, \ldots, 2^m - 1)$, the roles of $C_{S,1}$ and $C_{S,k}$ are first interchanged by connecting D_1 to $C_{S,k}$ and D_k to $C_{S,1}$. Next, capacitors $C_{S,k}$ and C_F are randomly swapped, using the pseudo-random control signal N. Thus, the iterative relation in (25), together with the expression for $V_{\widehat{RND}}$ in (21), can be utilized to estimate δC_k. Accordingly, in general, by repeating this calibration method for each capacitor $C_{S,M} (M = 1, \ldots, 2^m - 1)$, all capacitor-mismatch errors δC_M can be estimated using the iterative relation

$$\widehat{\delta C_M}\ (n+1) = \widehat{\delta C_M}\ (n) - \varepsilon V_{\widehat{RND}}. \tag{26}$$

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