Discrete-Time Modeling of Clock Jitter in Continuous-Time ΔΣ Modulators

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Abstract - **This paper proposes a simple, yet accurate, discrete-time modeling technique for simulating the performance degradation in continuous-time ΔΣ modulators due to clock jitter. The proposed technique is based on the impulse-invariant transform and is applicable to modulators that employ non-return-to-zero (NRZ) or delayed return-to-zero (RZ) rectangular feedback pulses. It is also independent of both the loop transfer function of the ΔΣ modulator and the power spectrum of the clock jitter. Furthermore, a versatile clock generator is modeled in SIMULINK for accurate behavioral simulation of digital-to-analog converters (DACs) with arbitrarily-jittered rectangular pulses. This clock generator is used to confirm the accuracy and performance advantages of the proposed modeling technique**.

I. Introduction

Continuous-time (CT) ΔΣ modulators (Fig. 1) benefit from a number of architectural advantages over their discrete-time (DT) counterparts (Fig. 2), including: a greater potential for low-power and high-speed operation, and inherent suppression of both aliasing and sampling errors. The principal disadvantage of CT architectures is their high sensitivity to clock jitter [1]. Clock jitter introduces errors into both the forward path (as *sampling errors* at the quantizer input) and the feedback path (as *time-delay errors* in the DAC feedback pulses). Sampling errors are subject to the same noise shaping as quantization errors and, therefore, are insignificant to the overall performance. However, DAC time-delay errors are not suppressed by the ΔΣ loop-filter gain, and are the focus of this paper.

Accurate CT analysis of jitter-induced DAC time-delay errors often requires excessively long simulation times. While a number of methods have been proposed to reduce this simulation time, published results have either been specific to NRZ-type feedback pulses [2] [3] or have relied upon numerical methods [1].

This paper introduces a simple DT technique for the rapid, yet accurate, simulation of the time-delay errors generated in the feedback path of CT ΔΣ modulators, due to clock jitter. The proposed DT modeling technique is based on the impulse-invariant transform, which is a standard design tool for CT ΔΣ modulators. It can be easily applied to modulator architectures employing non-return-to-zero (NRZ) or return-to-zero (RZ) rectangular pulses in the feedback DAC. The proposed technique is more flexible than previously-reported methods, as it is independent of the loop transfer function of the ΔΣ modulator and the power spectrum of the clock jitter.

This paper also proposes a clock-generator model for simulating the effect of arbitrarily-jittered clock pulses in CT ΔΣ modulators using SIMULINK. The proposed clock generator allows for accurate behavioral simulation of DACs with arbitrarily-jittered rectangular pulses in CT ΔΣ modulators. These simulations are subsequently used to evaluate the effect of jitter-induced errors and, thus, validate the accuracy of the proposed DT technique for modeling DAC time-delay errors.

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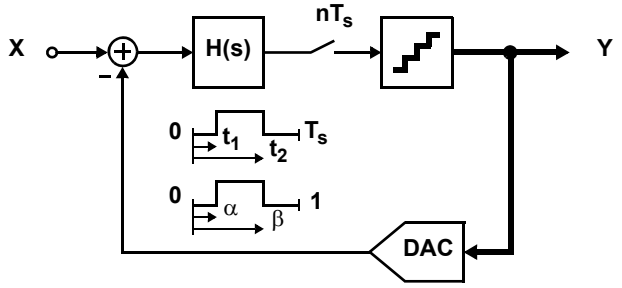

Fig. 1. Continuous-time ΔΣ modulator.

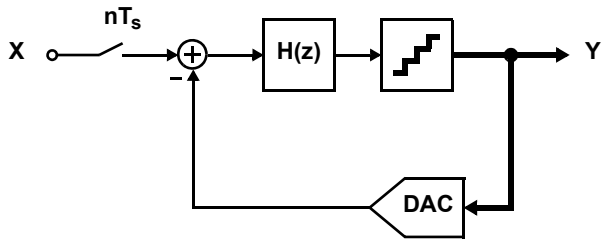

Fig. 2. Discrete-time ΔΣ modulator.

This paper is structured as follows: Section II proposes a DT technique for modeling DAC time-delay errors due to clock jitter. Section III develops a clock-generator model in SIMULINK. In Section IV, the DT modeling technique is validated by comparing its simulation results with those obtained through accurate simulation of CT ΔΣ modulators using the developed clock generator. Simulation performance advantages are also demonstrated.

II. Discrete-Time Modeling Technique

This section proposes a DT technique for the rapid behavioral simulation of the effect of jitter-induced time-delay errors in the DAC feedback path of CT ΔΣ modulators. To model CT timing errors in the DT domain, a set of *z*-domain mapping functions are developed. These mapping functions translate *time-delay errors* in the DAC feedback of a CT ΔΣ modulator into *coefficient errors* in the loop transfer function of its equivalent DT ΔΣ modulator.

This paper considers only rectangular feedback pulses, which are referred to using the naming conventions illustrated in Fig. 1. Here, α represents the delay between time $t = 0$ (the start of the sampling period) and time $t = t_1$ (the rising edge of the feedback pulse). Similarly, β represents the delay between time $t = 0$ and time $t = t_2$ (the falling edge of the feedback pulse). Both α and β are normalized with respect to the sampling clock period T_s. Observe that using this notation, an ideal NRZ pulse with an excess loop delay τ_d will have $\alpha = \tau_d / T_s$ and $\beta = 1 + \tau_d / T_s$ [1].

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A. Second-Order Example

Consider a DT loop transfer function $H(z)$. To develop its equivalent CT loop transfer function $H(s)$ using the impulse-invariant transform, the first step is to split the z-domain transfer function into its constituent terms by way of a partial fraction expansion. Equation (1) provides an example of a second-order term that may result from such an expansion:

$$H_2(z) = \frac{k_2}{(z-1)^2} \tag{1}$$

The goal here is to modify $H_2(z)$ such that it accounts for the effect of DAC time-delay errors in a CT ΔΣ modulator that employs the equivalent loop transfer function $H_2(s)$. Using α and β to represent the start and end times of the rectangular CT feedback pulse (Fig. 1), $H_2(z)$ can be transformed into the s-domain, using the impulse-invariant transform [1], as:

$$H_2(s) = \frac{r_{21}(sT_s) + r_{22}}{(sT_s)^2} \tag{2}$$

where $r_{21} = \frac{1}{2}\frac{k_2(\alpha+\beta-2)}{(\beta-\alpha)}$ and $r_{22} = \frac{k_2}{(\beta-\alpha)}$

Assume that the clock edges α and β (Fig. 1) are perturbed by, respectively, errors $\Delta\alpha$ and $\Delta\beta$ due to clock jitter. Define:

$$\widehat{\alpha} \equiv \alpha + \Delta\alpha \text{ and } \widehat{\beta} \equiv \beta + \Delta\beta \tag{3}$$

Then, $H_2(s)$ in equation (2) can be converted back into the z-domain, using the inverse impulse-invariant transform with $\widehat{\alpha}$ and $\widehat{\beta}$, as:

$$\widehat{H}_2(z) = \frac{c_{21}}{(z-1)} + \frac{c_{22}z + c_{23}}{(z-1)^2} \tag{4}$$

where $c_{21} = r_{21}(\widehat{\beta} - \widehat{\alpha})$

$$c_{22} = \frac{1}{2}r_{22}[\widehat{\beta}(2-\widehat{\beta}) - \widehat{\alpha}(2-\widehat{\alpha})]$$

$$c_{23} = \frac{1}{2}r_{22}(\widehat{\beta}^2 - \widehat{\alpha}^2)$$

The expression for $H_2(z)$ in equation (4) can be rewritten as:

$$\widehat{H}_2(z) = \frac{c_{21}+c_{23}}{(z-1)} + \frac{c_{22}+c_{23}}{(z-1)^2} = \frac{k_2}{(z-1)^2} + \frac{\Delta k_{22}}{(z-1)^2} + \frac{\Delta k_{21}}{(z-1)} \tag{5}$$

where Δk_{21} and Δk_{22} are defined in Table 1.

The first term in $\widehat{H}_2(z)$ represents the nominal component and is equal to $H_2(z)$ in equation (1). The second and third terms in $\widehat{H}_2(z)$ represent errors introduced by $\Delta\alpha$ and $\Delta\beta$ due to clock jitter. Therefore, $\widehat{H}_2(z)$ in equation (5) maps time-delay errors introduced in the DAC feedback pulses of a CT ΔΣ modulator into coefficient errors in the loop transfer function of its equivalent DT modulator, which was the stated objective.

The above DT modeling technique may be explained intuitively as follows. Using the nominal terms α and β in the $z \to s$ impulse-invariant transform (equation (2)) reflects the ideal design process. Subsequent introduction of time-delay errors $\Delta\alpha$ and $\Delta\beta$ (equation (3)) in the DAC feedback pulses results in a mismatch between the CT transfer function $H(s)$ and the original DT transfer function $H(z)$. This mismatch may be modeled in the discrete-time domain by performing the $s \to z$ impulse-invariant transform using nonideal delay terms $\widehat{\alpha}$ and $\widehat{\beta}$ (equation (5)).

B. Mapping Functions and Discrete-Time Simulations

Table 1 lists mapping functions for modeling the effect of time-delay errors in first, second, and third-order transfer-function terms with poles at the origin ($z = 1$) and with first-order poles at z_p. These functions were derived using the procedure described above.

Table 1. Mapping functions for modeling the effect of time-delay errors $\Delta\alpha$ and $\Delta\beta$ in the discrete-time domain.

Original Term	Time-Delay Error Mapping Function
$H_1(z) = \frac{k_1}{(z-1)}$	$\widehat{H}_1(z) = \frac{k_1}{(z-1)} + \frac{\Delta k_{11}}{(z-1)}$ $\Delta k_{11} = k_1(\Delta\beta - \Delta\alpha)(\beta-\alpha)^{-1}$
$H_2(z) = \frac{k_2}{(z-1)^2}$	$\widehat{H}_2(z) = \frac{k_2}{(z-1)^2} + \frac{\Delta k_{22}}{(z-1)^2} + \frac{\Delta k_{21}}{(z-1)}$ $\Delta k_{22} = k_2(\Delta\beta - \Delta\alpha)(\beta-\alpha)^{-1}$ $\Delta k_{21} = -(1/2)k_2(\Delta\alpha + \Delta\beta)$
$H_3(z) = \frac{k_3}{(z-1)^3}$	$\widehat{H}_3(z) = \frac{k_3}{(z-1)^3} + \frac{\Delta k_{33}}{(z-1)^3} + \frac{\Delta k_{32}}{(z-1)^2} + \frac{\Delta k_{31}}{(z-1)}$ $\Delta k_{33} = k_3(\Delta\beta - \Delta\alpha)(\beta-\alpha)^{-1}$ $\Delta k_{32} = -(1/2)k_3(\Delta\alpha + \Delta\beta)$ $\Delta k_{31} = (1/12)k_3[(\beta-\alpha)(\Delta\beta - \Delta\alpha) + 3(\Delta\alpha + \Delta\beta)]$
$H_{1p}(z) = \frac{k_{1p}}{(z-z_p)}$	$\widehat{H}_{1p}(z) = \frac{\Delta k_{11p} \cdot k_{1p}}{(z-z_p)}$ $\Delta k_{11p} = (z_p^{\beta-\Delta\alpha} - z_p^{\alpha-\Delta\beta})(z_p^{\beta} - z_p^{\alpha})^{-1}$

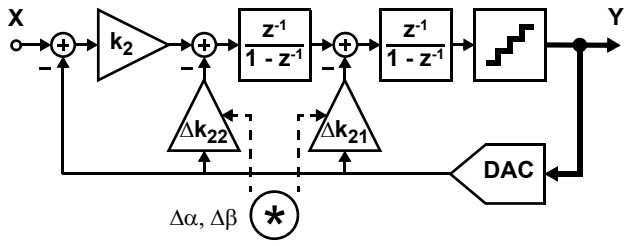

Fig. 3. Implementation of the $\widehat{H}_2(z)$ term in Table 1.

The mapping functions in Table 1 can be used for the DT simulation of jitter-induced time-delay errors in CT ΔΣ modulators, as follows:

1) If starting with a prototype DT loop transfer function $H(z)$ (Fig. 2), perform a partial-fraction expansion of $H(z)$.
   If starting with a CT loop transfer function $H(s)$ (Fig. 1), perform an $s \to z$ impulse-invariant transformation to obtain the equivalent DT transfer function $H(z)$, then perform a partial-fraction expansion of $H(z)$.
2) Replace each term in $H(z)$ with the equivalent mapping function in Table 1 to obtain $\widehat{H}(z)$.
3) Implement $\widehat{H}(z)$ in a DT ΔΣ modulator and simulate using a general-purpose simulator (e.g. SIMULINK).

Observe that in a CT ΔΣ modulator, the time-delay errors introduced by the DAC originate in the feedback path and, hence, are independent of the input signal path. For correspondence with the CT case, $\widehat{H}(z)$ in Table 1 must therefore be implemented in a DT ΔΣ modulator architecture such that its coefficient errors Δk only affect the feedback path, and not the input signal path. Figure 3 provides an example implementation of the second-order term $\widehat{H}_2(z)$.

C. Advantages

The proposed DT modeling technique has the following advantages:

1) **Simulation Time and Accuracy:** The technique can be used to rapidly simulate the effect of jitter-induced DAC timing errors in CT ΔΣ modulators, while maintaining a high-degree of accuracy, as demonstrated in Section IV.
2) **Jitter Power Spectrum:** Time-delay errors $\Delta\alpha$ and $\Delta\beta$ have classically been modeled using normally-distributed white noise sources [1]. The proposed technique, however, is not specific to a jitter spectrum.
3) **DAC Feedback Pulses:** The proposed technique provides accurate results for both NRZ and RZ rectangular feedback pulses, as demonstrated in Section IV.
4) **Continuous-Time ΔΣ Modulator Architecture:** Accurate simulations of various CT ΔΣ modulators were performed for both feedforward and distributed-feedback architectures. Results showed that jitter sensitivity is equivalent whether a loop transfer function is implemented using a feedforward or a distributed-feedback architecture. This equivalence remained even when DACs with uncorrelated errors were used in the distributed-feedback architecture. Accordingly, at the system level, jitter sensitivity is only a function of the loop transfer function $H(s)$. Hence, the proposed DT modeling technique will provide accurate results, independent of the architectural implementation of the corresponding CT loop transfer function $H(s)$.

III. Jittered-Clock Generation in SIMULINK

To validate the proposed DT modeling technique, a versatile clock generator was developed in SIMULINK to simulate the effect of arbitrarily-jittered clock pulses in CT ΔΣ modulators. The goal was to implement a simple system that would allow for realistic and, hence, accurate simulation of jitter effects, while allowing for full control over the timing of the generated pulse edges. This clock-generator model is then used to simulate both RZ and NRZ DACs with arbitrarily-jittered rectangular pulses in CT modulators.

A. SIMULINK Implementation

Rather than using the CT delay blocks in SIMULINK, which do not provide sufficient accuracy, the clock generator was implemented entirely in DT. Its building blocks are divided into two sampling domains: 1) a *nominal-resolution domain*, operating at the sampling period T_s; and 2) a *high-resolution domain*, operating at a period of T_s/N_r. Here, integer N_r determines the pulse-edge resolution, as it sets the minimum realizable time-delay variations.

Generation of $\widehat{\alpha}$ and $\widehat{\beta}$

The SIMULINK blocks in Fig. 4(a) and (b) are used, respectively, to generate integers *A* and *B*, which represent the timing of the α and β clock edges. These blocks operate in the nominal-resolution domain T_s. The first three blocks set the delays of the generated clock edges, which correspond to $\widehat{\alpha}$ and $\widehat{\beta}$ (equation (3)). Here, the random number generators are initialized with mean values equal to the nominal α and β, and with standard deviations equal to the normalized clock jitter σ_α/T_s and σ_β/T_s (all multiplied by the pulse-edge resolution N_r). The saturation blocks are then used to limit the generated $\widehat{\alpha}$ and $\widehat{\beta}$ to $\alpha\pm2\sigma_\alpha/T_s$ and $\beta\pm2\sigma_\beta/T_s$, in order to prevent unrealistically large jitter.

In Fig. 4(a), the last two blocks process the integer $\widehat{\alpha}$ to generate two values for *A*: 1) a version of $\widehat{\alpha}$ delayed by one clock period; and 2) a version of $\widehat{\alpha}$ offset by N_r. Later, when generating the jittered clock using the SIMULINK block in Fig. 4(c), as described below, the values of *A* are compared with the output of a counter (with limits 0 and N_r-1). Thus, the value of *A* selected in Fig. 4(c) corresponds to the delayed value of $\widehat{\alpha}$ if $\widehat{\alpha}>0$ and to the offset value of $\widehat{\alpha}$ if $\widehat{\alpha}<0$. Accordingly, the value of $\widehat{\alpha}$ is effectively generated one clock cycle earlier in order to handle the case where negative jitter results in $\widehat{\alpha}<0$ (i.e. when the α edge of the current clock cycle appears during the previous clock cycle).

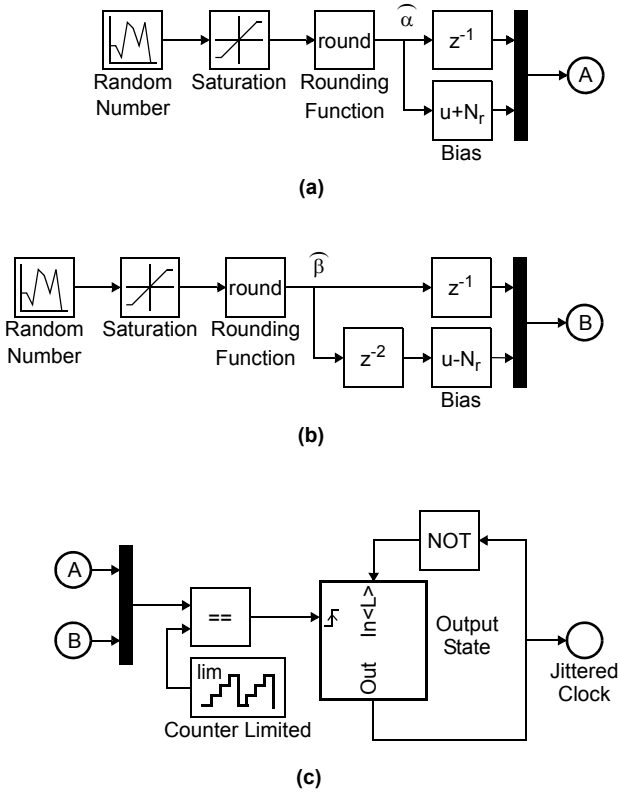

Fig. 4. Block diagrams of the SIMULINK clock generator. Here, the blocks are used to generate: **(a)** the α edge timing (operating at T_s); **(b)** the β edge timing (operating at T_s); and **(c)** the jittered clock (operating at T_s/N_r).

In Fig. 4(b), the values of *B* are generated in a similar manner as for *A*. However, rather than dealing with previous and current clock cycles as in the case of *A*, the *B* blocks are concerned with the current and next clock cycles.

Note that it is assumed that clock jitter does not force the α edges into the next clock cycle or the β edges into the previous clock cycle.

Generation of the Jittered Clock

In Fig. 4(c), the SIMULINK blocks operate in the high-resolution domain T_s/N_r. These blocks translate the *A* and *B* integers (generated in Fig. 4(a) and (b)) into edge timing for the jittered clock at the output of the clock generator. This is achieved through a comparison with a limited counter, as described above. The result is a series of impulses, which act as the clock signal for an output flip-flop. This flip-flop is important to avoid problems that may arise from an unintentional overlap of α and β terms, effectively causing each edge to be indistinguishable from one another. Proper timing is guaranteed by ensuring that the first α edge occurs prior to the first β edge.

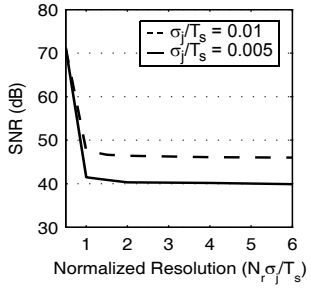

Fig. 5. SNR versus normalized pulse-edge resolution ($N_r\sigma_j/T_s$) for Architecture 1 in Table 2.

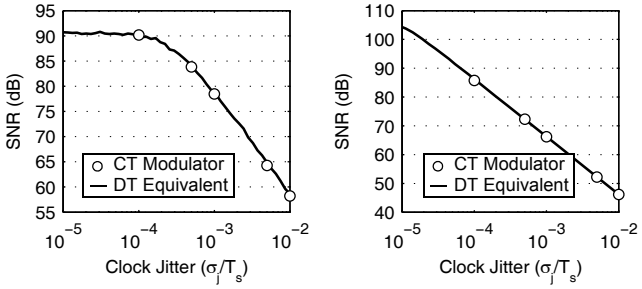

Fig. 6. SNR versus normalized clock jitter (σ_j/T_s) of a CT modulator (based on the developed clock generator) and of its equivalent DT modulator (based on the proposed DT modeling technique) for: **(a)** Architecture 1; and **(b)** Architecture 2 in Table 2.

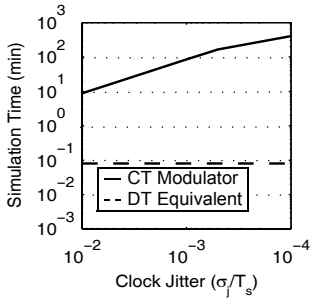

Fig. 7. Simulation time versus normalized clock jitter (σ_j/T_s) for the results reported in Fig. 6(a).

Table 2. Continuous-time ΔΣ modulator test architectures.

Arch.	Loop Transfer Function	Properties
1 [4]	$H_A(s) = \frac{r_{21}(sT_s)+r_{22}}{(sT_s)^2+z_p^2} + \frac{r_1}{(sT_s)}$	OSR = 16, Bits = 5 NRZ DAC $\alpha = 0.50$, $\beta = 1.50$
2	$H_B(s) = \frac{r_3}{(sT_s)^3} + \frac{r_2}{(sT_s)^2} + \frac{r_1}{(sT_s)}$	OSR = 32, Bits = 5 RZ DAC $\alpha = 0.25$, $\beta = 0.75$

DACs with Jittered Rectangular Pulses

To model an NRZ DAC, the output of the proposed clock generator (Fig. 4) is used as the clocking signal for a standard flip-flop, with α set equal to the normalized excess loop delay τ_d/T_s and β initialized to ensure that $\beta > \alpha$. To model an RZ DAC, the output of the proposed clock generator is used both as the clocking signal and the active-low reset for a standard flip-flop, with α and β set equal to the normalized clock-edge times (Fig. 1).

B. Pulse-Edge Resolution

The pulse-edge resolution variable N_r determines the minimum time-delay variation realizable using the proposed clock generator (Fig. 4). Since the clock output stage in Fig. 4(c) operates at a sampling period of T_s/N_r, any increase in N_r will result in a proportional decrease in the maximum simulation step size. This will increase the simulation accuracy, at the expense of simulation time.

To determine the minimum pulse-edge resolution N_r required for accurate simulation, Architecture 1 in Table 2 was simulated using the proposed clock generator. Figure 5 depicts the signal-to-noise ratio (SNR) at the modulator output versus the normalized pulse-edge resolution $N_r\sigma_j/T_s$ of the generated clock pulses for variable normalized jitter σ_j/T_s, assuming Gaussian-distributed clock jitter with $\sigma_\alpha = \sigma_\beta = \sigma_j$. Accordingly, a resolution N_r of $2T_s/\sigma_j$ allows for sufficient accuracy, irrespective of σ_j.

IV. Simulation Results

Table 2 specifies the loop transfer function, oversampling ratio *OSR*, number of quantization bits, and DAC properties for two third-order CT ΔΣ modulators. Observe that this choice of loop transfer function $H(s)$ ensures that all terms in Table 1 are tested.

A. Accuracy of Discrete-Time Technique

The loop transfer functions in Table 2 were simulated in SIMULINK using: 1) a CT ΔΣ modulator based on the developed clock generator (with $N_r = 2T_s/\sigma_j$) to model the DACs with jittered rectangular pulses; and 2) an equivalent DT ΔΣ modulator based on the proposed DT modeling technique.

Figure 6 compares the SNR at the modulator output versus normalized clock jitter σ_j/T_s, assuming Gaussian-distributed clock jitter with $\sigma_\alpha = \sigma_\beta = \sigma_j$. The excellent matching (to within 1-dB) between the accurate CT and the equivalent DT simulations in Fig. 6 confirms the accuracy of the proposed DT modeling technique.

B. Simulation Time

Figure 7 compares the time required for the CT and DT simulations reported in Fig. 6(a). Observe that, as the magnitude of the normalized jitter variation σ_j/T_s decreases, the required pulse-edge resolution ($N_r = 2T_s/\sigma_j$) increases, proportionally increasing the required simulation time for the CT ΔΣ modulator. However, the required simulation time for the equivalent DT ΔΣ modulator is constant, as it is independent of the magnitude of the jitter variation. Furthermore, even for the smallest value of σ_j/T_s (largest value of N_r), the time for DT simulations is over an order of magnitude smaller than that for CT simulations. This demonstrates the performance achievements of the proposed DT modeling technique.

V. Conclusion

A discrete-time modeling technique was proposed to rapidly, yet accurately, simulate the effect of clock jitter in the DAC feedback path of a continuous-time ΔΣ modulator. The proposed technique is applicable to any type of rectangular feedback pulse and is not specific to either the jitter power spectrum or ΔΣ modulator architecture. Furthermore, a versatile continuous-time clock generator was developed in SIMULINK to directly model DACs with arbitrarily-jittered rectangular pulses. This clock generator was subsequently used to validate the proposed discrete-time modeling technique. Behavioral simulation results confirm both the accuracy and the improved simulation performance of the proposed discrete-time technique.

VI. References

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