Behavioral Modeling of Opamp Gain and Dynamic Effects for Power Optimization of Delta-Sigma Modulators and Pipelined ADCs

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ABSTRACT

This paper proposes a simple, yet accurate, analytical model for the effect of opamp gain and dynamics (slew rate and bandwidth) on the transfer function of switched-capacitor (SC) amplifiers and integrators. Furthermore, it demonstrates the detrimental effects of: a) the nonlinear variation in the opamp dc gain; and b) the feedforward transmission of the feedback capacitor, on the harmonic distortion and settling behavior of these SC stages.These effects, typically ignored in the behavioral simulations of SC stages, are analyzed and modeled. Thus, accurate behavioral simulations of ΔΣ modulators or pipelined analog-to-digital converters (ADCs) can be performed in SIMULINK, using the proposed models for their SC building blocks (integrators or amplifiers). The proposed behavioral models are validated in HSPICE. Behavioral simulation examples are presented to illustrate the importance of such accurate modeling for low-power design.

Categories and Subject Descriptors: B.7.1 [Integrated Circuits]

General Terms: Design, Performance, Theory

Keywords: Behavioral modeling, synthesis, discrete-time systems, analog-to-digital conversion, sigma-delta (ΣΔ) modulation.

1. INTRODUCTION

Switched-capacitor (SC) integrators and amplifiers (Fig. 1) are the basic building blocks of ΔΣ modulators and pipelined ADCs, respectively. One of the most challenging aspects in the behavioral simulation of an SC stage (amplifier or integrator) is the modelling of the circuit nonidealities in its opamp. Accordingly, this paper proposes an analytical model for the behavioral simulation of the effect of opamp gain and dynamics on the gain of an SC amplifier and the transfer function of an SC integrator.

Several tools for the high-level synthesis and behavioral simulation of pipelined ADCs [1] and ΔΣ modulators [2,3] have been developed. However, this paper focuses on modeling specific building blocks (amplifiers and integrators) for behavioral simulations in the widely-used and versatile SIMULINK tool. The goal is to develop analytical models which are reasonably accurate, while being simple, tractable, and meaningful to circuit designers (*only circuit-design parameters, no empirical values*).

Several SIMULINK-based models for the behavioral simulation of the gain of an SC amplifier [4] or the transfer function of an SC integrator [5,6] have been previously reported. Opamp dynamics in SC integrators have also been previously modeled [7]. However, in modeling the opamp circuit nonidealities and feedback-system behavior, many of these previously-reported models did not account for: a) the nonlinear variations in the opamp dc gain with its output voltage; and/or b) the feedforward transmission of the feedback capacitor C_F in an SC stage (Fig. 1).

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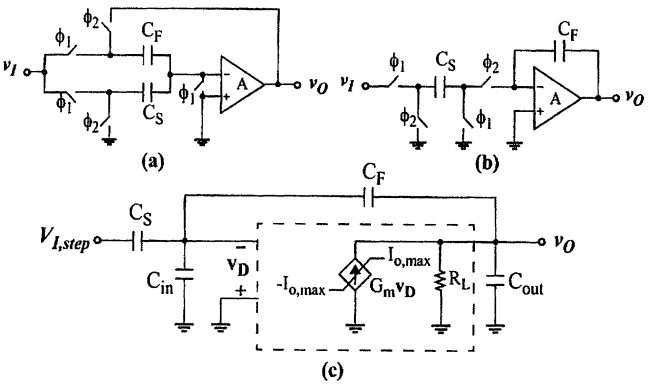

Fig. 1 (a) SC amplifier; (b) SC integrator; c) Configuration of (a) and (b) during the charge-transfer clock phase ϕ_2, with the opamp equivalent-circuit model shown. Here, C_S and C_F are the sampling and feedback capacitors; C_{in} and C_{out} are the total capacitances, including any parasitic, at the opamp's input and output nodes.

Both of these effects have a detrimental impact on the opamp settling behavior and harmonic distortion in an SC stage, especially when designing for low-power in nano-scale CMOS technologies (Section 6.2). In this paper, these effects are analyzed and modeled.

Accordingly, in Section 2, this paper develops a feedback model for an SC stage during its charge transfer phase. In Sections 3 and 4, it models the effect of the following opamp nonidealities on the transfer function of SC stages (Fig. 1):

1) finite dc gain A_0
2) nonlinear variations in dc gain A_0 with output voltage v_O
3) limited output-signal swing (output saturation voltage V_{Osat})
4) dynamic effects (finite bandwidth ω_{3dB} and slew rate SR)
5) parasitic capacitances (C_{in} and C_{out})
6) feedforward transmission of feedback capacitor C_F

In Section 5, SIMULINK models for SC amplifiers and integrators are proposed. In Section 6, simulation results are presented to validate the proposed behavioral models and demonstrate the importance of using these models for the accurate behavioral simulation and, hence, power optimization of ADCs.

2. EQUIVALENT FEEDBACK MODEL

2.1 Open-Loop Opamp Characteristics

The following analysis assumes a dominant-pole load-compensated opamp with a first-order transfer function

$$A(s) \equiv A_0/(1+s/\omega_p) \quad (1)$$

where $A_0 \equiv G_m R_L$ and $\omega_p \equiv 1/(R_L C_L)$ are the opamp's open-loop dc gain and dominant pole, respectively. Here, G_m is the short-circuit transconductance, R_L is the equivalent load resistance, and C_L is the equivalent load capacitance of the opamp (Fig. 1c).

2.2 Closed-Loop SC-Stage Characteristics

Consider an SC stage, as configured during its charge-transfer phase (Fig. 1c). During this clock phase, the feedback capacitor C_F provides not only signal feedback, but also signal feedforward.

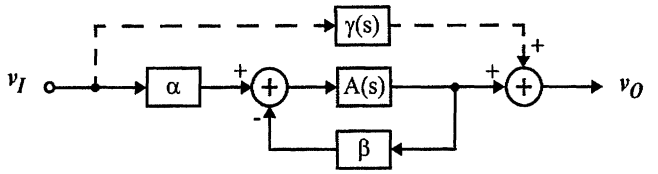

Fig. 2 Equivalent feedback model of an SC stage during its charge-transfer phase (Fig. 1c): a) series-shunt model (γ=0); b) return-ratio model (forward transmission γ modeled).

Typically, a *series-shunt feedback model* is used to represent the SC stage during its charge-transfer phase. This corresponds to the feedback model in Fig. 2, *without* the feedforward path (dashed line). Hence, in a series-shunt feedback model, the forward transmission due to feedback capacitor C_F is neglected compared to the larger forward transmission of the opamp [8]. However, this leads to detrimental modeling inaccuracies (Section 6.2.2).

In this paper, a *return-ratio feedback model* is utilized to more accurately model an SC stage during its charge-transfer phase. This corresponds to the feedback model in Fig. 2, with the feedforward path (dashed line) utilized to account for the forward transmission $\gamma(s)$ due to feedback capacitor C_F [9]. Accordingly, by considering the definitions and equivalent circuit of each term in the return-ratio feedback model, the closed-loop transfer function of the SC stage (Fig. 1c) can be expressed as:

$$A_{CL}(s) \equiv \frac{\alpha A(s)}{1+\beta A(s)} + \gamma(s) = \alpha_0 K \frac{(1-s/\omega_z)}{(1+s/\omega_{3dB})} \qquad (2)$$

α	$= C_S/(C_S+C_{in}+C_F)$	*Forward Factor*
β	$= C_F/(C_S+C_{in}+C_F)$	*Feedback Factor*
α_0	$= (A_0\beta)/(1+A_0\beta)$	*Gain Factor due to Finite A_0*
K	$= C_S/C_F = \alpha/\beta$	*Nominal Capacitor Ratio*
ω_{3dB}	$= \beta\,(G_m/C_L)/\alpha_0$	*Closed-Loop Dominant Pole*
ω_Z	$= G_m/C_F$	*Closed-Loop Transmission Zero*
C_L	$= C_{out}+\beta(C_S+C_{in})$	*Equivalent Open-Loop Load Cap.*

Hence, the forward transmission $\gamma(s)$ due to feedback capacitor C_F introduces a transmission zero ω_Z in the transfer function.

3. OPAMP DYNAMICS

Consider an SC stage, as configured during its charge-transfer phase (Fig. 1c). Its step response depends on the step response of its opamp. As depicted in Fig. 3, the opamp step response typically includes a slewing (nonlinear settling) region due to finite slew rate SR, followed by a linear settling region due to finite bandwidth ω_{3dB}. In the following, the closed-loop step response $v_O(t)$ of the SC stage is derived, assuming a step voltage of height $V_{I,step}$ is applied at its input at time $t = 0$.

3.1 Linear Settling

During linear settling, the opamp output approaches its final value exponentially. Here, the step response of the SC stage is

$$V_O(s)|_{LIN} = \frac{V_{I,step}}{s} A_{CL}(s) \qquad (3)$$

where $A_{CL}(s)$ is the closed-loop transfer function in (2). By taking the inverse-Laplace transform of (3), the step response of the SC stage can expressed in the time domain as

$$v_O(t)|_{LIN} = v_O(0^-) + V_{O,step}\,[1 - K_Z\, e^{-t/\tau}] \qquad (4)$$

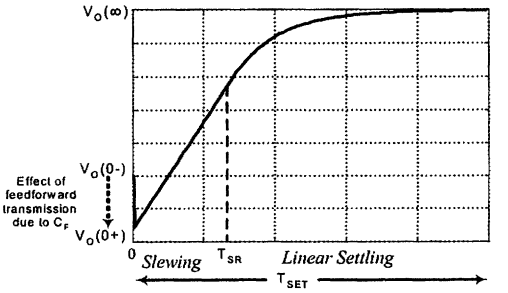

Fig. 3 Typical settling behavior of an SC stage in its charge-transfer phase (Fig. 1c), when a step voltage is applied at its input.

Here,

$V_{O,step}$	$\equiv v_O(\infty) - v_O(0^-) = \alpha_0 K V_{I,step}$	*Nominal Output Step*
K_Z	$\equiv 1 + \omega_{3dB}/\omega_Z$	*Transmission-Zero Factor*
τ	$\equiv 1/\omega_{3dB}$	*Closed-Loop Time Constant*

where $v_O(0^-)$ is the value immediately before $t = 0$ and $v_O(\infty)$ is the asymptotic final value of the opamp output.

Based on equation (4), the value of the opamp output immediately after $t = 0$ is

$$v_O(0^+) = v_O(0^-) + (1 - K_Z) V_{O,step} \qquad (5)$$

Therefore, at the start of the charge-transfer phase, since $K_Z > 1$, the feedforward transmission due to feedback capacitor C_F causes a step change in the output in a direction opposite to its final value (Fig. 3). Hence, the *actual* output change required for complete settling is increased from $|V_{O,step}|$ to $|K_Z V_{O,step}|$. The resulting adverse effect on the settling and distortion errors is shown in Section 6.2.2.

3.2 Slewing

During slewing (nonlinear settling), the maximum rate at which the opamp output changes is limited by its slew rate SR. Here, the step response of the SC stage is

$$v_O(t)|_{SR} = v_O(0^+) + SR_0\, t \qquad (6)$$

where $SR_0 \equiv SR \cdot sign(V_{O,step})$ to account for both rising and falling outputs.

3.3 Slewing followed by Linear Settling

Assume that the opamp step response has a slewing behavior followed by linear-settling (Fig. 3), as is typically the case in an SC stage. Let T_{SR} denote the slewing period. Then,

- For $0 < t \le T_{SR}$: slewing occurs. Hence, the step response is

$$v_O(t)|_{SR/LIN} = v_O(0^+) + SR_0\, t \qquad (7)$$

- For $t \ge T_{SR}$: linear settling occurs and the output approaches $v_O(\infty)$ exponentially. Hence, the step response is

$$v_O(t)|_{SR/LIN} = v_O(T_{SR})|_{SR}\, e^{(T_{SR}-t)/\tau} + v_O(\infty)[1 - e^{(T_{SR}-t)/\tau}] \qquad (8)$$

Based on the condition of continuity of the derivatives of $v_O(t)|_{SR/LIN}$ in (7) and (8) at $t = T_{SR}$, the slewing period is

$$T_{SR} = \frac{K_Z |V_{O,step}|}{SR} - \tau \qquad (9)$$

Observe that, during linear settling, the maximum slope of the step response in (4) occurs at $t = 0$ and has a value of $K_Z|V_{O,step}|/\tau$. Therefore, slewing occurs if $K_Z|V_{O,step}|/\tau > SR$.

3.4 Modeling of Opamp Dynamics in SC Stages

In an SC stage, opamp dynamics cause errors in charge transfers between capacitors, during the charge-transfer phase. Let T_{SET} denote the settling period (the time available for charge transfer). Let $v_O(n)$ denote the output of the SC stage, *assuming no opamp dynamic limitations*. To account for opamp dynamics, the output of the SC stage must be expressed as $\hat{v}_O(n)$ with

- if $\frac{K_Z|V_{O,step}|}{\tau} < SR$ (no slewing): $\hat{v}_O(n) = v_O(T_{SET})|_{LIN}$ (10)
- else if $T_{SR} > T_{SET}$ (only slewing): $\hat{v}_O(n) = v_O(T_{SET})|_{SR}$ (11)
- else (slewing+linear): $\hat{v}_O(n) = v_O(T_{SET})|_{SR/LIN}$ (12)

Here, index n denotes time $t = n\,T_S$, where T_S is the clock period.

4. NON-LINEAR OPAMP DC GAIN

In a CMOS opamp, the dc gain varies with the output voltage due to the dependency of the output resistance r_{ds} of a MOS transistor on its drain-to-source voltage v_{DS}. The nonlinear variations in the opamp dc gain A_0 can be modeled as a function of the opamp output voltage v_O using [10]:

$$A_0(v_O) = \begin{cases} A_{0max}\left[1-\left(\frac{v_O}{V_{Osat}}\right)^2\right] & \text{for } v_O \le V_{O,sat} \\ 0 & \text{for } v_O > V_{O,sat} \end{cases} \quad (13)$$

where A_{0max} is the maximum dc gain and V_{Osat} is the output saturation voltage of the opamp. In the behavioral modeling of an SC stage (in Section 5), equation (13) will be utilized to express the dc gain A_0 as a function of the SC-stage output voltage $\hat{v}_O(n)$.

5. BEHAVIORAL MODELING OF SC STAGES

The output of an SC amplifier (Fig. 1a) can be expressed as

$$v_O(n) = \alpha_0\,(1+K)\,v_I\left(n-\frac{1}{2}\right) \quad (14)$$

Here, $1+K = 1+C_S/C_F$ is the amplifier gain and $v_I(n)$ is the amplifier input. The parameter α_o, as defined in (2), is the gain error due to the opamp's finite nonlinear dc gain A_0.

The output of an SC integrator (Fig. 1b) is expressed as [10]:

$$v_O(n) = \alpha_0\,K\,v_I(n-1) + \beta_0\,v_O(n-1) \quad (15)$$

where

$$\beta_0 = \alpha_o\left[1+\frac{(1+C_{in}/C_F)}{A_0}\right] \quad (16)$$

Here, $K = C_S/C_F$ is the integrator gain and $v_I(n)$ is the integrator input. Parameter α_o, as defined in (2), is the gain factor and parameter β_0 is the phase factor (shifted pole frequency) in the SC integrator, due to its opamp's finite nonlinear dc gain A_0.

Accordingly, the SIMULINK block models in Fig.4 and Fig. 5 can be utilized for the behavioral simulation of SC amplifiers (Fig. 1a) and integrators (Fig. 1b), respectively. They account for the effects of all opamp nonidealities listed in Section 1 on the amplifier gain in (14) and on the gain and phase of the integrator transfer function in (15), as described above.

In Fig. 4 and Fig. 5:

- The function block *opamp_gain* computes the opamp dc gain A_0 as a function of the SC stage output $\hat{v}_O(n)$, as per equation (13). The function blocks *alpha_0* and *beta_0* compute, respectively, α_o and β_o based on A_0 and the SC stage capacitances, as per equations (2) and (16).
- A saturation (limiter) block is placed at the SC stage output to model the output saturation level V_{Osat} of its opamp.
- The function block labelled *SR/BW* models the opamp dynamics, as per expressions (10)-(12). Its input variables are $v_O(n)$, $v_O(0^-)$, and α_o. Observe that:
  - In an SC amplifier, the output is reset during the sampling phase. Therefore, $v_O(0^-) = 0$ is used in Fig. 4.
  - In an SC integrator, capacitor C_F is not reset during the sampling phase, but holds the previous integration-phase charge. Therefore, $v_O(0^-) = \hat{v}_O(n-1)$ is used in Fig. 5. The SIMULINK model in Fig. 5 models a non-inverting, delaying SC integrator. For a non-delaying integrator, simply delete the delaying block at the integrator input. For an inverting integrator, replace gain K with $-K$.

6. BEHAVIORAL SIMULATION RESULTS

6.1 Gain Error

Assume a step voltage of height $V_{I,step}$ is applied at the input of an SC stage during its charge-transfer phase (Fig. 1c). With an ideal opamp, the resulting change at the output is $K\,V_{I,step}$. Therefore, the gain error of the SC stage can be defined as

$$\delta g \equiv 1 - \frac{v_O(T_{SET}) - v_O(0^-)}{K\,V_{I,step}} \quad (17)$$

Typically, the step response of an SC stage is characterized by slewing followed by linear settling. Therefore, the gain error can be expressed, using (8) and (17), as

$$\delta g = \frac{1}{1+\beta A_0} + \frac{SR\tau}{KV_{I,step}}\,e^{(T_{SR}-T_{SET})/\tau} \quad (18)$$

Observe that the left-hand term accounts for the gain error due to the opamp finite gain, while the right-hand term represents the gain error due to the opamp dynamics (finite bandwidth and slew rate).

To validate the accuracy of the proposed behavioral models, the equivalent circuit model in Fig. 1c was simulated in HSPICE, with the opamp's slew rate modeled by limiting the maximum current of its transconductance G_m. The initial output voltage was set to zero.

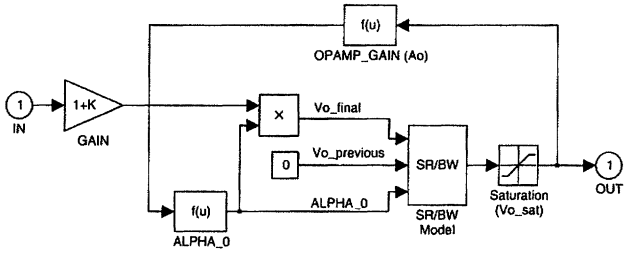

Fig. 4 SIMULINK model of an SC amplifier (Fig. 1a).

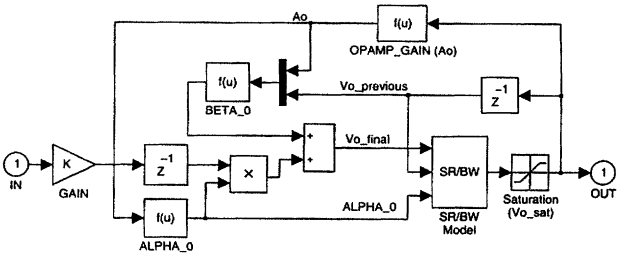

Fig. 5 SIMULINK model of a non-inverting delaying SC integrator (Fig. 1b)

Fig. 6 shows the results for δg versus $V_{I,step}$, computed based on HSPICE simulations and on the proposed behavioral models in equation (18). The excellent agreement between these results confirms the accuracy of the proposed behavioral models.

6.2 ADC Power Optimization

6.2.1 Opamp Nonlinear DC Gain vs. Harmonic Distortion

Consider a 3rd-order 5-bit ΔΣ modulator, with its noise transfer function having 1 zero at dc and 2 complex-conjugate zeros optimally placed within the signal band [11]. The modulator was simulated in SIMULINK with its 1st integrator modeled using the proposed behavioral model (Fig. 5), while the 2nd and 3rd integrators were assumed to be ideal.

Fig. 7 shows the signal-to-noise-plus-distortion ratio (SNDR) of the ΔΣ modulator versus the maximum dc gain A_{0max} of its opamp, when: a) the dc gain is constant ($A_0 = A_{0max}$); and b) the dc gain varies nonlinearly with the opamp output, as per (13). Accordingly, when designing using moderate-gain opamps (~50dB), the SNDR is significantly degraded (>8dB) due to nonlinear dc-gain variations. Thus, the effect of nonlinear dc gain cannot be neglected in behavioral simulations, especially when designing using moderate gain opamps: For example, in nano-scale CMOS technologies, high dc gains for the opamps are difficult to achieve at low power, due to the low supply voltages and the poor intrinsic gains of the MOS transistors.

6.2.2 Feedforward Transmission of C_F vs. Power Dissipation

A 2nd-order 1-bit ΔΣ modulator was simulated in SIMULINK, with its 1st integrator modeled using the proposed behavioral model (Fig. 5) to account for the opamp nonidealities. Assume:

- opamp's short-circuit transconductance: $G_m = I_{BIAS}/V_{OV}$
- opamp's slew rate: $SR = I_{BIAS}/C_L$;
- integrator closed-loop time constant: $\tau = (C_L/\beta)(V_{OV}/I_{BIAS})$

where I_{BIAS} is the opamp bias current and V_{OV} is the overdrive voltage of the opamp transistors. Accordingly, by expressing τ and SR in terms of I_{BIAS} in the proposed models, behavioral simulations can be performed to find the optimum I_{BIAS} required to achieve a given linearity and resolution.

Fig. 8 shows the modulator SNDR versus its opamp bias current I_{BIAS}, with: a) $K_Z = 1$ to neglect the effect of feedforward transmission due to the feedback capacitor C_F; and b) $K_Z = 1 + \omega_{3dB}/\omega_Z$. Accordingly, the estimated I_{BIAS} for achieving a given SNDR can be significantly underestimated and, more drastically, the modulator can be unstable when biased at this estimated current level. For example, with the effect of feedforward transmission due to C_F modeled, behavioral simulations show that a normalized $I_{BIAS} = 1$ is required to achieve an SNDR = 71 dB. Furthermore, a normalized $I_{BIAS} \geq 0.75$ is required to ensure that the ΔΣ modulator is stable. However, behavioral simulations with $K_Z = 1$ would have erroneously predicted that a normalized $I_{BIAS} = 0.45$ is sufficient to achieve an SNDR = 71dB, while in practice the ΔΣ modulator is unstable at this bias-current level.

7. CONCLUSION

The effects of opamp gain and dynamics on SC amplifier gain and SC integrator transfer function were analyzed and modeled. SIMULINK models of SC amplifiers and integrators were also developed and validated using HSPICE simulations. It was shown that the nonlinear dc gain variations in the opamp and the feedforward transmission of the feedback capacitor in an SC stage, typically ignored in the behavioral simulations of SC stages, have detrimental effects on the harmonic distortion and settling behavior. SIMULINK simulation results were presented to show the need for the proposed accurate models in low power design.

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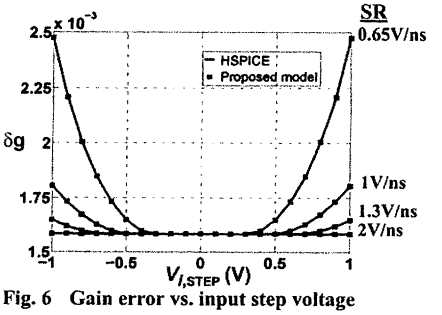

Fig. 6 Gain error vs. input step voltage for various SR values (C_S=C_F=C_{out}=2pF; C_{in}=0.2pF; R_L=200kΩ; G_m=10mA/V).

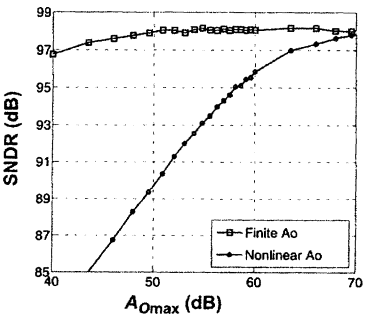

Fig. 7 SNDR vs. maximum dc gain A_{0max}

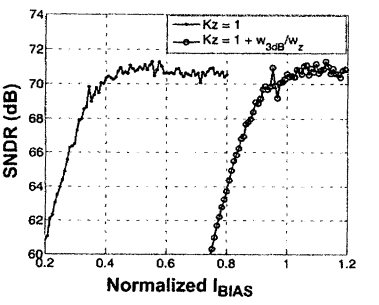

Fig. 8 SNDR vs. normalized bias current I_{BIAS}