Digital Background Calibration of a 0.4-pJ/step 10-bit Pipelined ADC without PN Generator in 90-nm Digital CMOS

Mohammad Taherzadeh-Sani and Anas A. Hamoui

Department of Electrical & Computer Engineering, McGill University, Montreal, Canada (anas.hamoui@mcgill.ca)

ABSTRACT

In nanometer digital CMOS, the linearity of pipelined A/D converters (ADCs) is degraded by the low dc gains of the opamps. Gain-enhancement techniques significantly increase the analog-circuit design complexity at low power and low voltage. Therefore, even in medium-resolution applications, digital background correction is attractive for designing power-efficient ADCs. A simple, yet accurate, digital background calibration technique, which does not require a pseudo-random (PN) calibration signal, is proposed to minimize the power dissipation in the digital calibration unit. It achieves the same convergence speed and accuracy as PN-based techniques in 2-path (split) pipelined ADCs. A 10-bit 44-MS/s pipelined ADC, fabricated in a standard 1.2-V 90-nm digital CMOS process, uses the proposed calibration technique to achieve a 58.7-dB SNDR for a 21.5-MHz input, with a figure-of-merit (FOM) of 0.4 pJ/step.

I. INTRODUCTION

The linearity of a pipelined analog-to-digital converter (ADC) is primarily degraded by linearity errors in its pipeline stages. In a switched-capacitor pipeline stage, the primary sources of linearity errors are: a) gain errors in the residue amplifier, due to the low dc gains of the opamps; and b) nonlinearity in the digital-to-analog sub-converter (sub-DAC), due to capacitor-mismatch errors.

For medium-resolution (< 10 bits) pipelined ADCs, adequate capacitor matching is readily obtainable in standard nanometer CMOS processes. However, in these scaled processes, high dc gains for the opamps are not easily realizable at low power, due to the low supply voltages and the low intrinsic gains of the MOS transistors.

To design power-efficient pipelined ADCs in nanometer CMOS processes, one approach is to build high-gain opamps using: a) special high-performance analog transistors (however, this requires additional processing steps and, hence, higher fabrication costs) [1]; or b) analog gain-enhancement techniques (however, this increases the analog circuit-design complexity and the time-to-market) [2]. Another approach, followed in this paper, is to calibrate the pipeline stages for gain errors. Digital background calibration is the most attractive technique, as it does not require high-resolution analog circuitry, it is portable across technologies and benefits from technology scaling, it is robust to environmental changes, and it does not interrupt the normal operation of the ADC. Although digital calibration is typically reserved for high-resolution applications, this paper demonstrates its power efficiency in the design of medium-resolution pipelined ADCs.

This paper describes a novel digital background calibration technique and its implementation in a 10-bit pipelined ADC with a split (2-path) architecture (Fig. 1). Fabricated in a standard 1.2-V 90-nm digital CMOS process, this ADC achieves a 58.7-dB SNDR (9.5-bit ENOB) for a 21.5-MHz input signal at a 44-MS/s sampling frequency, with a figure-of-merit of:

\[
\text{FOM} = \frac{\text{Power}}{\left(2^{\text{ENOB}} \cdot f_s\right)} = 0.4 \text{ pJ/step}
\]

Accordingly, it achieves a FOM comparable to the most power-efficient ADC [2], among the state-of-the-art 10-bit medium-speed (\(< 200\text{MS/s})\) pipelined ADCs fabricated in standard digital CMOS processes and measured at \(f_{in} = f_s/2\) [2-8].

II. PIPELINED ADC ARCHITECTURE

Pipelined ADCs with a split (2-path) architecture (Fig. 1) have been demonstrated to significantly reduce the calibration time of PN-based calibration techniques, without increasing the chip area and power consumption compared to their classical (1-path) equivalents [10,11]. This paper assumes that the 1st pipeline stage in each path of the 2-path pipelined ADC is a 1.5-bit residue stage (Fig. 2).
A mismatch between the transfer functions of paths verified experimentally (Section IV). The validity of this assumption will be low dc gains of the opamps in the pipeline stages and both paths use this assumption, as most of the gain error is due to the zero-mean noise errors, added to the ADC input signal in paths and . In the following, an input reference voltage ( in Fig. 2) is assumed for simplicity.

III. PROPOSED CALIBRATION TECHNIQUE

A. Gain-Error Estimation

To simplify the calibration algorithm, assume that the 1st pipeline stages in paths and have the same gain error : \( \delta g = \delta g_a = \delta g_b \) (4) This is a reasonable assumption, as most of the gain error is due to the low dc gains of the opamps in the pipeline stages and both paths use the same opamp design. The validity of this assumption will be verified experimentally (Section IV).

Constant dc gains and can be added (Fig. 2) to create a mismatch between the transfer functions of paths and . Figure 3 depicts the input-output transfer functions of the 1st pipeline stages in paths and, when:

\[ R_a = 1/8 \quad \text{and} \quad R_b = -1/8 \] (5)

It can be shown that these constant signals do not affect the ADC functionality, if \( R_a \) and \( R_b \) are less than 1/4 [10].

Assume that the residue signals \( y_a \) and \( y_b \) are perfectly digitized as \( Y_a \) and \( Y_b \) by the subsequent pipeline stages in Fig. 1 (the back-end ADCs in Fig. 2). Then:

\[ Y_a = (2x_a - D_a) V_{ref}(1 - \delta g) \quad \text{and} \quad Y_b = (2x_b - D_b) V_{ref}(1 - \delta g) \] (6)

where \( \Delta y_a \) and \( \Delta y_b \) are offset errors, due to the 1st pipeline stage and the back-end ADC in paths and , respectively.

Step 1 When \( D_a = D_b \):

This corresponds to regions ii and iv of the pipeline-stage transfer curves in Fig. 3, where \( D_a - D_b = 0 \). Therefore, equation (8) simplifies to

\[ Y_b - Y_a = 2(x_b - x_a) - (D_b - D_a)(1 - \delta g) + (\Delta y_b - \Delta y_a) \] (8)

Define a signal error \( E \) as the average of \( Y_b - Y_a \).

Then, substituting (1) into (9) and taking the average:

\[ E = Y_b - Y_a = 2(\Delta x_b - \Delta x_a)(1 - \delta g) + (\Delta y_b - \Delta y_a) \] (9)

The signal error \( E \) will be used to estimate gain error \( \delta g \).

Step 2 When \( D_a \neq D_b \):

This corresponds to regions i, iii, and v of the pipeline-stage transfer curves in Fig. 3, where \( D_a - D_b \neq 0 \). Therefore, equations (6), (7), and (10) can be combined and simplified to:

\[ (Y_b - Y_a) - E = [2(N_b - N_a) + 1](1 - \delta g) \] (11)

Taking the average of equation (11) leads to:

\[ (Y_b - Y_a) - E = 1 - \delta g \] (12)

Therefore, the gain error can be estimated as:

\[ \delta g = 1 - (Y_b - Y_a) - E \] (13)

B. Gain-Error Correction

A non-zero gain error \( \delta g \) affects the digitized residue signals \( Y_a \) and \( Y_b \), as per equations (6) and (7). Let \( Y_{a,\text{cal}} \) and \( Y_{b,\text{cal}} \) denote the calibrated values of \( Y_a \) and \( Y_b \), with the effect of \( \delta g \) removed. Assuming \( \delta g^2 \ll \delta g \), these can be computed in the digital domain as:

\[ Y_{a,\text{cal}} = Y_a(1 + \delta g) \quad \text{and} \quad Y_{b,\text{cal}} = Y_b(1 + \delta g) \] (14)

These calibrated residue signals are then passed to the digital error-correction block, which generates the ADC output.

C. Summary of Calibration Steps

Figure 4 summarizes the proposed digital background calibration algorithm for the 2-path ADC (Fig. 2):

- When \( D_a = D_b \), update signal error \( E \), using equation (10).
- When \( D_a \neq D_b \), update gain error \( \delta g \), using equation (13).
- Digitally calibrate residue signals \( Y_a \) and \( Y_b \), using equation (14).
- Pass the calibrated residue signals \( Y_{a,\text{cal}} \) and \( Y_{b,\text{cal}} \) to the digital error-correction block to compute the ADC output.
D. Comparison to PN-based Digital Calibration Techniques

Compared to previously-reported PN-based methods for the digital background calibration of 2-path pipelined ADCs [10,11], the proposed technique differs as follows:

1) Calibration Signals \( R_a \) and \( R_b \): In PN-based methods, \( R_a \) and \( R_b \) are two different pseudo-random (PN) binary signals. This requires a PN-signal generator and additional analog and digital circuits to apply the time-varying PN signals to the pipeline stages. Using the proposed calibration technique, this extra circuitry is not required, as the calibration signals have constant dc values (\( R_a \) and \( R_b \)).

2) Gain Errors \( \delta g_a \) and \( \delta g_b \): In PN-based calibration methods, the gain error is calibrated separately for each path. In the proposed calibration technique, the gain errors are assumed to be equal in both paths (\( \delta g = \delta g_a = \delta g_b \)) for simplicity. The validity of this assumption will be verified experimentally under worst-case conditions (Section IV).

IV. EXPERIMENTAL RESULTS

The proposed calibration technique is implemented in a 2-path pipelined ADC. Each path is a 10-bit pipelined ADC, consisting of eight 1.5-bit pipeline stages followed by a 2-bit flash ADC. As the ADC performance is most sensitive to the 1st pipeline stage in each path, only these stages are calibrated.

Owing to the digital gain calibration, the dc-gain requirements are relaxed on the opamps in the pipeline stages. Hence, the opamps are designed using a simple two-stage configuration (which has a good noise performance, simple biasing, and large output-voltage swing). Furthermore, owing to the digital error correction, the offset requirements are relaxed on the comparators in the sub-ADCs of the pipeline stages. Hence, the implemented design uses dynamic comparators.

A. Experimental Test Setup

One path of the 2-path pipelined ADC has been fabricated in a standard 1.2-V 90-nm digital CMOS process (Fig. 10). To realize the 2-path ADC, two ADC chips are then mounted on two identically-designed PCBs (Fig. 5). Both PCBs are then driven by the same analog-input and clock signals, but with calibration signals \( R_a \) and \( R_b \) applied to PCBs \( A \) and \( B \), respectively. The proposed calibration technique is implemented in MATLAB.

By fabricating only one path of the 2-path ADC and utilizing this experimental test setup (Fig. 5), significant savings in chip area and, hence, fabrication cost are achieved for the ADC prototype. Furthermore, by implementing each path on a different die, the worst-case mismatch between gain errors \( \delta g_a \) and \( \delta g_b \) is present. This allows us to experimentally verify our hypothesis (equation (4)) that gain errors \( \delta g_a \) and \( \delta g_b \) can be assumed equal for the purpose of gain calibration, even under worst-case matching conditions.

B. Dynamic and Static Performance

Figure 6 shows the output spectrum of the calibrated 2-path ADC for a 21.5-MHz input signal sampled at 44 MS/s. The SNDR is 58.7 dB (9.5-bit effective resolution). The 3rd-order harmonic is below -68 dB, resulting in a 68-dB SFDR.

Figure 7 shows the measured SNDR of the 2-path ADC versus input-signal frequency, with and without calibration. The sampling frequency is 44 MS/s. Accordingly, the SNDR is improved by 4dB, using the proposed calibration technique. Furthermore, an SNDR of more than 58 dB is achieved across the full input-frequency range (250 kHz - 21.5 MHz).

Figure 8 shows the INL and DNL of the calibrated 10-bit 2-path ADC, sampled at 44-MS/s sampling frequency. The INL and DNL are less than 1 LSB and 0.8 LSB, respectively.
C. Convergence Accuracy and Speed

In our ADC prototype chip, calibration signals $R_a$ and $R_b$ were made available off-chip, in order to test calibration techniques with different $R_a$ and $R_b$. Figure 9 compares the convergence speed of the proposed calibration technique (with $R_a = 1/8$ and $R_b = 1/8$) and the previously-reported PN-based calibration technique in [10-11] (where $R_a$ and $R_b$ are two uncorrelated PN binary signals). Accordingly, both techniques show the same convergence speed, requiring about $10^5$ samples to converge to within 1dB of the final SNDR. Furthermore, the final SNDR values reached using both techniques are within 1dB. This confirms that the proposed calibration technique achieves the same performance (convergence speed and accuracy) compared to previously-reported PN-based methods, while being simpler to implement (Section III).

D. Power Dissipation

To estimate the power dissipation when using the proposed digital calibration technique, the digital calibration unit has been synthesized and made available off-chip, in order to test calibration techniques with different $R_a$ and $R_b$. SNDR values during the normal ADC operation, using:

TABLE I   Measured Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>90-nm standard digital CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Supply</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Full-Scale Analog Input</td>
<td>1.4 V_f</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 bits</td>
</tr>
<tr>
<td>Sampling Rate ($f_s$)</td>
<td>44 MS/s</td>
</tr>
<tr>
<td>SNDR @ $f_{in}$=21.5MHz</td>
<td>58.7 dB</td>
</tr>
<tr>
<td>Analog Power @ $V_{DD}$ = 1.2 V</td>
<td>3.4 mW</td>
</tr>
<tr>
<td>Digital Power @ $V_{DD}$ = 1.2 V</td>
<td>3.4 mW</td>
</tr>
<tr>
<td>FOM = Power/(2SNDR in bits $f_{in}$)</td>
<td>0.4 pJ/step</td>
</tr>
</tbody>
</table>

TABLE II Performance Comparison of 10-bit Pipelined ADCs, measured at $f_{in}$=21.5MHz in standard digital CMOS.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS (nm)</th>
<th>$f_D$ (V)</th>
<th>$f_{in}$ (MHz)</th>
<th>Power (mW)</th>
<th>SNDR (dB)</th>
<th>Calibrate</th>
<th>FOM (pJ/step)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISSCC05 [8]</td>
<td>180</td>
<td>1.8</td>
<td>125</td>
<td>40</td>
<td>53.7</td>
<td>No</td>
<td>0.79</td>
</tr>
<tr>
<td>ISSCC05 [7]</td>
<td>90</td>
<td>1.2</td>
<td>12</td>
<td>3.3</td>
<td>52.6</td>
<td>No</td>
<td>0.76</td>
</tr>
<tr>
<td>ISSCC06 [6]</td>
<td>90</td>
<td>1.2</td>
<td>100</td>
<td>35</td>
<td>56.7</td>
<td>No</td>
<td>0.6</td>
</tr>
<tr>
<td>JSSC07 [5]</td>
<td>90</td>
<td>1.0</td>
<td>100</td>
<td>33</td>
<td>55.3</td>
<td>No</td>
<td>0.69</td>
</tr>
<tr>
<td>JSSC06 [4]</td>
<td>90</td>
<td>1.2</td>
<td>200</td>
<td>54.6</td>
<td>53.6</td>
<td>No</td>
<td>0.7</td>
</tr>
<tr>
<td>JSSC07 [3]</td>
<td>180</td>
<td>1.8</td>
<td>50</td>
<td>11</td>
<td>34.6</td>
<td>No</td>
<td>0.5</td>
</tr>
<tr>
<td>ISSCC07 [2]</td>
<td>90</td>
<td>1.2</td>
<td>80</td>
<td>13.3</td>
<td>35.6</td>
<td>Yes</td>
<td>0.34</td>
</tr>
<tr>
<td>This work</td>
<td>90</td>
<td>1.2</td>
<td>44</td>
<td>12.2</td>
<td>58.7</td>
<td>Yes</td>
<td>0.4</td>
</tr>
</tbody>
</table>

VI. REFERENCES