Wafer Post-Processing for a Reconfigurable Wafer-Scale Circuit Board

Moufid Radji[1], Ahmed Lakhssassi[2], Mohammed Bougataya[2], Anas Hamoui[1], Ricardo Izquierdo[3]

(1) Electrical and Computer Engineering Department, McGill University
(2) Département d'Informatique et d'Ingenierie, Université du Quebec en Outaouais
(3) Département d'Informatique, Université du Quebec à Montréal

Abstract

The WaferBoard™ rapid prototyping platform for electronic systems is proposed as a tool to help meet today's tight delivery time, performance and reliability constraints. At the core of WaferBoard™ is the WaferIC™, a wafer-scale reconfigurable CMOS circuit. At the surface of this complex circuit is a sea of identical contacts, any pair of which can be interconnected through a mesh grid network called WaferNet™. The user can simply deposit packaged integrated circuits on the smart active surface, and then a complex interconnect pattern between these ICs can be established in a matter of minutes. As is the case with development of any novel technology, design of the platform poses several technical challenges. Postprocessing tasks to be accomplished on the CMOS wafer are laid out hereafter. A .18µm CMOS TestChip fabricated to validate the WaferIC™ concept on a 1/100th scale is outlined. Furthermore, sample microfabrication results, such as TSV etching, are presented along with thermo-mechanical investigation outcomes.

Key words: Electronic Prototyping, Wafer-Scale Integration, Through Silicon Vias, Thermo-Mechanical Analysis

I. INTRODUCTION

In the recent years, electronic devices have been required to provide an ever-growing set of functionality. As the field of circuit design is relatively mature, pressure to deliver these full-featured electronic systems is increasingly born by the systems engineer. At the prototyping stage several iterations of a complex interconnection network often need to be implemented, each requiring the tedious and time consuming redesign of a Printed Circuit Board (PCB). To meet the tight constraints on size, power efficiency and time-to-market, new techniques for prototyping of electronic systems need to be put in place. WaferBoard™[1], a rapid prototyping technology based on a wafer scale circuit, WaferIC™[1], is proposed to mitigate this development and prototyping bottleneck. The WaferIC sits on a bed of power-supply circuitry inside a robust mechanical housing. The WaferIC is an active substrate that can transmit digital information between any package balls of a set of conventional chips placed by the user (user ICs, or uICs) anywhere on its surface. The surface is alignment-insensitive, so hand-placement is sufficient. The WaferIC detects uIC contacts, and based on the package footprint and minimal user input, the WaferConnect™ software identifies the components present on the smart surface and provides power and ground to the uICs through the proper contact nodes. During a configuration step, the user specifies inter-chip connections which are downloaded thereafter in a manner similar to programming a Field Programmable Gate Array (FPGA). Signal paths contain repeaters to ensure signal integrity. The WaferIC provides connectivity to uICs on the top side, and to the power supply circuitry on the back side. Topside contacts to uICs are made through metal plated bumps on top of WaferIC™. The bumps are required to provide sufficient ductility and deformability to attain a good electrical contact. They must also offer good thermal transfer to maintain temperature homogeneity on WaferIC™ and uICs. Through-Wafer Vias (TWV) are used to feed the WaferIC from underneath directly into an internal WaferIC power distribution grid that starts on metal 1 (M1). Through silicon vias (TSVs) technology is currently under development [2], and figure 1 shows a sample etch result. However, unlike these samples, the TSV's required for the WaferBoard™ platform must be etched through the silicon from the backside and stop on the lowest metal layer of the standard CMOS process.

Characterization of key features in the fabrication of the WaferIC is being done on full size wafers; in addition a 2x1.9mm^2 .18µm CMOS chip, TestChip1.0, was fabricated through TSMC to

[1]WaferBoard™ is a brand name for a Rapid Prototyping Platform for Electronic Systems from Gestion TechnoCap Inc., DreamWafer Division.

validate functionality on a 1/100th scale. In this paper, the physical structure of WaferBoard^{TM} is first laid out, along with a description of some of the postprocessing challenges. Then focus is placed on TSVs, a key postprocessing step. Next is an overview of the Testchip1.0 along with preliminary investigations made on it. Lastly thermo-mechanical investigations undertaken so far are shown before concluding remarks.

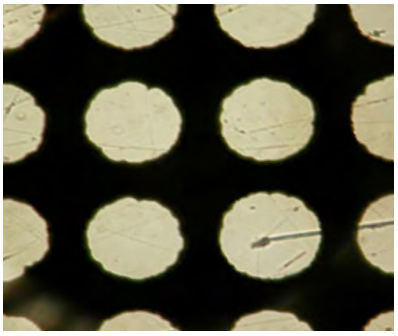


Figure 1: Optical image of backside illuminated TSVs: 200µm diameter-600µm thick wafer

II. PHYSICAL STRUCTURE OF WAFERBOARD^{TM}

A. Overview

The WaferBoard^{TM} platform is a reconfigurable circuit board whose main component is a wafer scale CMOS circuit, WaferIC. The physical housing is designed with a strong emphasis on heat and stress mitigation. Atop WaferIC is a pouch filled with thermally conductive fluid attached to the lid. The fluid not only dissipates heat through the top of the structure, but it also enables the application of uniform pressure onto the uICs which can have various heights. The applied pressure is controlled by a plunger which can generate up to 10 atmospheres, as needed to ensure proper detection and connection to the BGA-bumped uICs. The surface of the WaferIC consists of a very dense sea of contacts (NanoPad^{TM}) each capable of providing power or routing a signal from any pin of a uIC. Since the nanopads' size is much smaller, and their density is much higher than that of uIC BGA solder balls, each component contacts several nanopads at once. An internal wafer-scale interconnect network, WaferNet^{TM}, is used to link any two given nanopads, by carrying signals between them. Power for the WaferIC and the uICs is provided though a network of connections on the backside. By means of TSVs and solder bumps, the WaferIC is connected to the power supply assembly. The entire structure sits a on a backside heat sink which dissipates some of the heat through the bottom. Figure 2 depicts a schematic cross-section of the device.

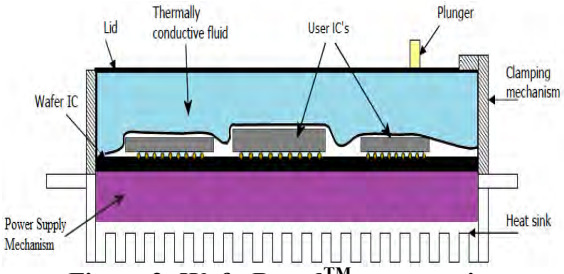


Figure 2: WaferBoard^{TM} cross-section

B. A few postprocessing challenges

The first and probably least trivial step is the design and fabrication of the wafer scale CMOS circuit. Besides all RTL and transistor level issues, one bottleneck comes from the limited reticule size. A characteristic of WaferIC that greatly helps with this is its repetitive cell-based architecture. The single building block is as cell containing an array of nanopads. WaferNet ensures the complex interconnections between these cells which are tiled on the reticule scale; reticule stitching techniques [1] are then used to obtain the wafer scale interconnect network.

After the circuit is manufactured by the CMOS foundry, several postprocessing steps still remain to be performed to attain a functional device.

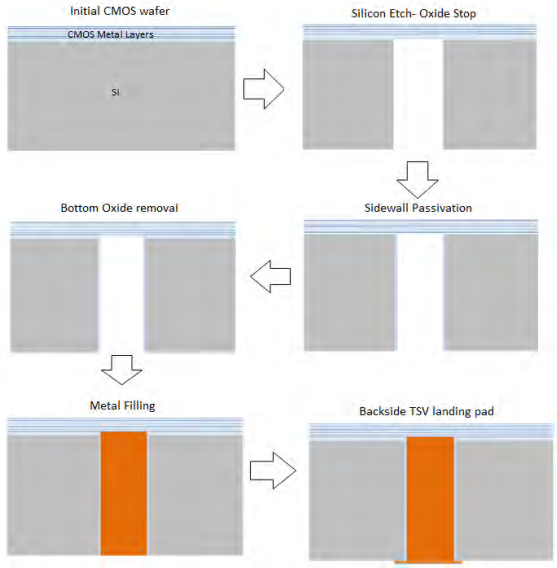


Figure 3: TSV process flow

On the top surface, gold columns up to 50µm in height have to be plated above each 80x80µm nanopad. A barrier layer such as nickel needs to first be deposited between the top layer aluminum and the gold columns. The columns' height is chosen to provide enough compliance to accommodate the small variability in BGA sizes underneath uICs by deforming the soft gold. On the bottom surface TSVs of aspect ratio 5:1 need to be etched and metal filled. In doing this, the oxide underneath metal 1 must be used as etch stop, similarly to the Buried Oxide layer (BOX) used on Silicon-on-Insulator (SOI) wafers for manufacturing of MEMS devices

such as accelerometers[3]. Figure 3 describes the process flow to be followed to attain these TSVs. Next, solder bumps are placed to provide connection to power supply assembly. Given the large number of contacts and the coarse nature of alignment done with bumping tools, this step will prove quite challenging[4].

III. TSVs, A KEY POSTPROCESSING STEP

A. TSV etching

Etching is to be done using an Inductively Coupled Plasma (ICP) tool capable of achieving Deep Reactive Ion Etching (DRIE). The standard Robert Bosch GmbH process is chosen to obtain deep trenches using the ICP-DRIE tool [3]. As the process results from cycling through an etch step followed by a deposition step, the Bosch process suffers from the scalloping effect; this effect along with the roughness of the sidewalls is clearly visible on figure 4. This rough surface may prove detrimental during the via filling step.

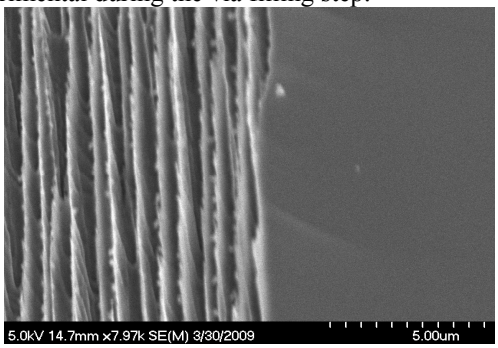


Figure 4: SEM image showing side wall roughness

Another characteristic of the process which can prove troublesome in some applications is its Aspect Ratio Dependant Etching (ARDE); figure 5 clearly illustrates this. Using the Bosch process, attempting to etch different via widths at the same depth using a single mask can be cumbersome.

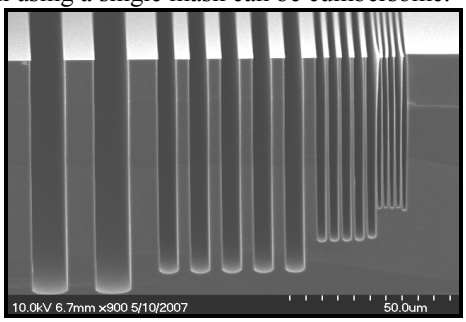


Figure 5: ARDE: 10um, 5um, 2um and 1um Openings *Courtesy of*: **Philippe Vasseur-***LMF-Ecole Polytechnique de Montreal*

In order to design a reliable recipe for etching through the 50µm-dia vias present on the testchip, several iterations had to be made on centimeter-size samples. Each such sample was covered with patterns for various via sizes and shapes. Figure 6 below describes the process flow used.

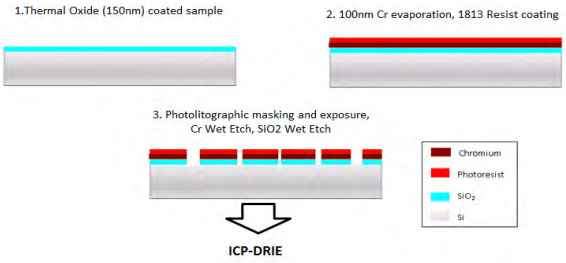


Figure 6: Bosch Process Characterization sample preparation

Initially, the recurring issue was the formation of "black silicon", at the bottom of the vias, which eventually halts the etching. Figure 7 shows these grass roots, which are due to overpassivation. The effective solution was found to be the significant increase of the etch step duration with respect to the passivation step. Figure 8 shows square vias with rounded corner, and figure 9 is a set of sample etch profiles obtained with the optimized recipe. As can be understood from table 1, this recipe is optimized for a given via width, and depth. In very narrow vias, the sidewall forms an acute angle with respect to the horizontal, whereas this angle is obtuse in very large openings. One can expect sidewall angle below 1 degree for the target 50um vias. The aspect ratio is not a linear function of width, rather the aspect ratio increases rapidly as the width decreases.

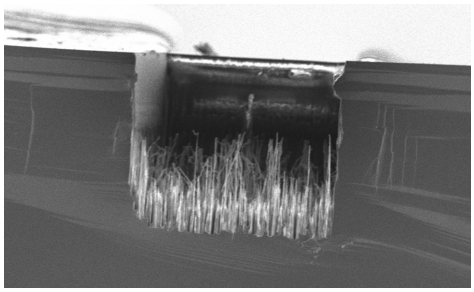


Figure 7: SEM Image showing black silicon issue

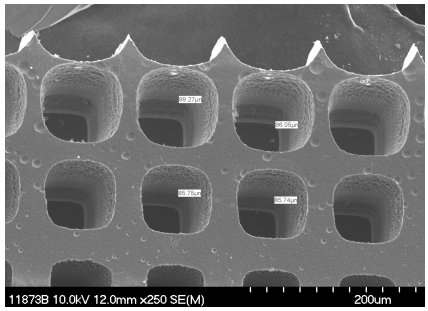


Figure 8: Sample Etching output, 45 degree angle view

C. Via filling

Once the vias have been successfully etched, the next task is to insulate their walls and metalize them to ensure connection of M1 to the backside landing pads.

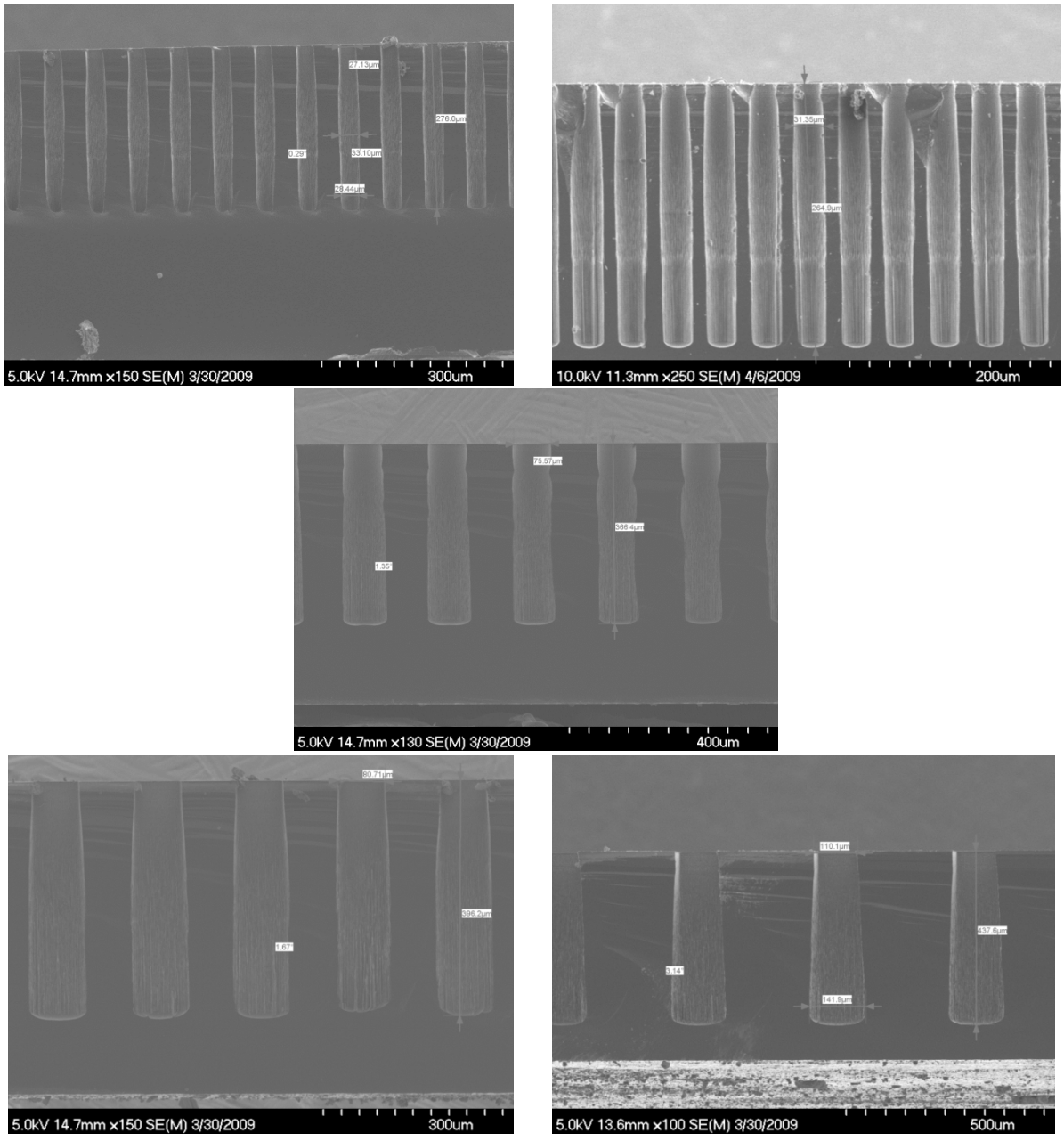


Figure 9: SEM profile of sample etch results

Width(μm)	**Depth**(μm)	**Aspect ratio**	**Sidewall Angle**(deg)
10	153	15.3	-1.26
30	269	8.97	0.29
40	316	7.9	0.88
80	381	4.8	1.51
110	437	4.0	3.14
200	496	2.5	4.24

Table 1: Summary of Etch results

Coating of a sidewall insulation dielectric is done to limit leakage current from any via into the silicon substrate. Achieving a conformal coating of SiO_2 while remaining below the CMOS temperature limit of 400ºC poses a few difficulties. In a conventional Low Pressure Chemical Vapor deposition (LPCVD) system, the thermal energy required for deposition dictates temperatures of 700ºC or higher. Other techniques of direct deposition suffer from line-of-sight limitations given the required depth of the vias. The envisaged solution to overcome the high temperature requirement of LPCVD is the use of plasma to enhance the chemical reaction (PECVD) at temperatures of 400ºC or lower. There is effectively a tradeoff between coating quality and deposition temperature. The source gas can be either Oxygen or Tetra-Ethyl-Ortho-Silicate (TEOS). Inductively coupling the plasma (ICPECVD)[7] has also proven to result in deposition of a quality film.

To remove the oxide underneath M1, dry etching has to be performed. The ICP-DRIE tool will be used with a proper combination of gases for selective etching of SiO_2. Given the highly uneven topologies, dry film resist will need to be used as masking layer for this step. Metal filling will then be done using standard electroplating techniques or simply a conductive paste as best suited for low contact resistance. Lastly the backside pad layer will be electroplated or patterned from a copper foil.

IV. TESTCHIP1.0

The Test-Chip1.0 on figure 10 is an array of 3x3 WaferIC unit cells each made of 4x4 nanopads. To the right of the active area is a column used for characterization of two postprocessing tasks: reticule stitching and TSVs. All around the chip are wire bonding pads used for packaging of the device. The entire circuit cover covers an area of $2x1.9mm^2$.

For electrical testing and validation, the chip is packaged using the wire bonding pads. For postprocessing, on the other hand, bare dies are utilized. The rightmost column consists of passive patterns, most of which serve the purpose of characterizing reticule stitching. Figure 11 below outlines the simple pattern used to emulate the overlap of metal lines for inter-reticule stitching[1].

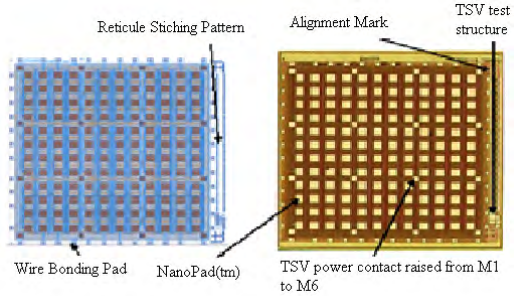
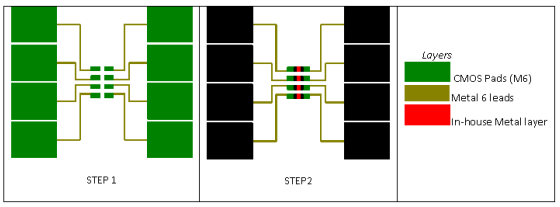
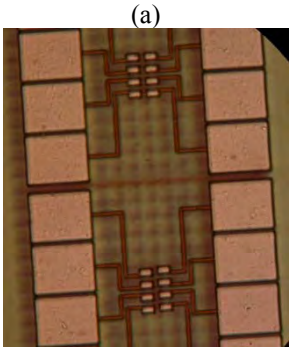


Figure 10: TestChip1.0 Layout and Micrograph



(a)



(b)

Figure 11: Inter-reticule stitching patterns (a) layout of process, (b) optical image of Step 1 pattern

Within the same column, a structure is designed to verify the attainment of M1 and the continuity of metal in the TSV. Besides this TSV characterization pattern, TestChip1.0 features 16 TSV connections pads on M1 of size 50x50µm in the active circuitry. For this test circuit, the power supply is routed to predetermined bonding pads, not just to TSVs as will be the case on the actual WaferIC. For probing purposes, the M1 TSV contact is raised to M6 through a series of vias. The FIB image on figure 12 shows a side view of the layer stack above a TSV. The oxide layer underneath M1 is apparent. Work is currently being done to apply the aforementioned etch recipe to TestChip1.0 using this oxide layer as etch-stop. A slight overetch will be performed to ensure silicon removal with minimal damage to the oxide layer due to the 150:1 selectivity to SiO_2[3]. Another useful feature of the designed recipe is the presence of a small amount of passivation gas present during the etch step, this help to reduce any notching effects [3].

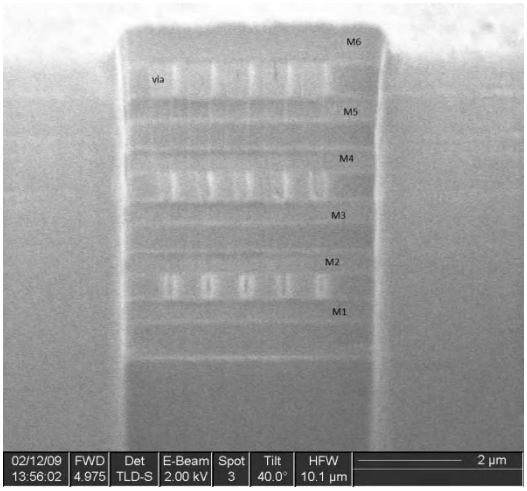


Figure 12: FIB slice of TSV top pad

V. THERMO-MECHANICAL ANALYSIS

The reduced feature sizes, increased power requirements and package contact densities all contribute to make thermal issues extremely critical in designing WaferBoard^{TM} platform. Thermal analysis is a crucial vehicle for predicting the change in the electrical characteristics or possible stress-induced failure of the platform. The complexity of the device dictates the need for a detailed analysis and optimization of coupling between both the heat-transfer fluid pouch used to apply even pressure on uICs, and to the backside heat sink through WaferIC and its supporting structures; i.e. the complete thermal coupling from components to ambient. The accurate and fast evaluation of heat flow patterns becomes an essential step in the overall design verification. This consists in studying a wide variety of possible thermal scenarios of operation of the WaferBoard^{TM} to obtain a preliminary assessment of its thermo-mechanical behavior.

A. Wafer Scale Thermal Analysis

In this section, the estimation of thermal peaks and the stress induced on the WaferIC^{TM} are presented. These have become a major issue with the ever increasing power density of uICs deposited on its surface. The investigation is done using a thermal heat sources placement approach to estimate and predict working temperature of WaferBoard^{TM} structures. In a second step, estimated temperature gradients are used to calculate stress profiles. Finite element analysis is used for peak temperature prediction during WaferBoard^{TM} operation. NISA finite element software (Numerical Integrated elements for System Analysis) [8] is used to predict thermal behavior. The power dissipated in heat sources (components) placed on the WaferIC^{TM} is modeled by heat flux produced inside the components. The final results are dependent on several parameters and thermo-mechanical components of the system, such as the uIC package and heat sinks (geometry and materials), to be designed at a later stage of this research. The main heat source is the uICs, and based on on-going detailed electrical design [9] the bulk of the power consumed by the WaferIC^{TM} is dissipated directly underneath these uICs. The specific benchmark for which results are presented in this paper is a 60W IC (a Pentium is used for reference) for which the package has a 40*40mm^2 area (0.0016 m^2). The problem formulation is presented graphically in figure 13.

Figure 14 shows the evolution of the temperature at Y1-Top solders balls- WaferIC^{TM}. Hence, a non-uniform temperature profile and thermal peaks of 42.2 ^oC exists through the device thickness at the Top solders balls- WaferIC^{TM} interface. Under these conditions, the maximum thermal variation ΔT_{max} is 17.2 ^oC in the structure.

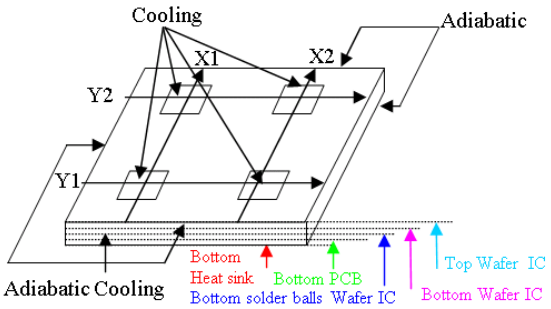


Figure 13: WaferBoard^{TM} inside thermal boundary condition (BC)

However, at the Top solders balls- WaferIC^{TM} interface the maximum local thermal variation $\Delta T_{max(loc)}$ is 3 ^oC induced locally during WaferIC powering. Between the components, there is subsequent relaxation on temperature gradients through the structure leading to an essentially uniform temperature variation. The cooling of the device is effectively controlled by conduction through to the WaferIC and through to the component.

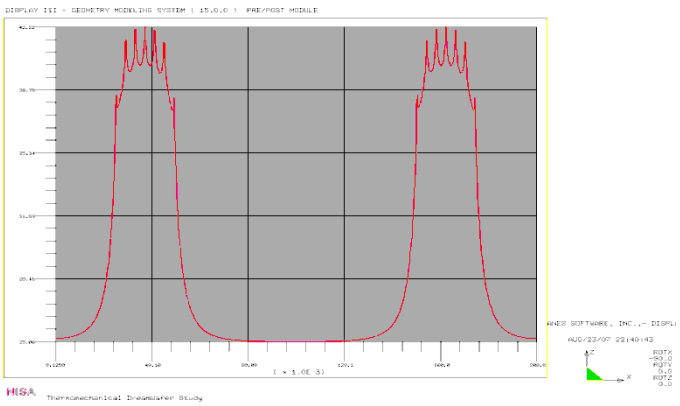


Figure 14: Sandwich forced convection through PCB surfaces Temperature profile Y1-Top solders balls- WaferIC^{TM}

B. Thermo-mechanical stress analysis of WaferIC in the presence of TSV's in 70 micron model

For stress analysis, the 70 micron thick model is used to obtain critical thermal and mechanical analysis data. Furthermore, a quarter model is designed to reduce the total number of finite elements and allow for a manageable sized model.

Multilevel structures with TSVs are becoming commonplace in the electronic industry. Because these structures are made of materials that have different properties, specifically a different coefficient of thermal expansion (CTE), thermal stresses, distortion, and warpage are a source of concern. In the case of thin multilayered devices with TSV such WaferIC, the surface may be assumed to be in a state of plane stress [10]. Hence, an extensive finite element analysis is needed to investigate the WaferIC surface, especially at solder balls interfaces. In this section, the approach proposed captures the thermo-mechanical stress singularity at the WaferIC level to predict the critical tensile stress. Thus, this approach is only valid for steady-state heat conduction and is limited by simplifying assumptions. Hence, predicted hot spot temperature and realistic associated stress distribution can be used to guide thermo-mechanical design. Figure 15 shows shear stress results in the Y1-Bottom solders balls-WaferIC interface in the case of sandwich forced convection through PCB surfaces and simply supported in the bottom boundary conditions.

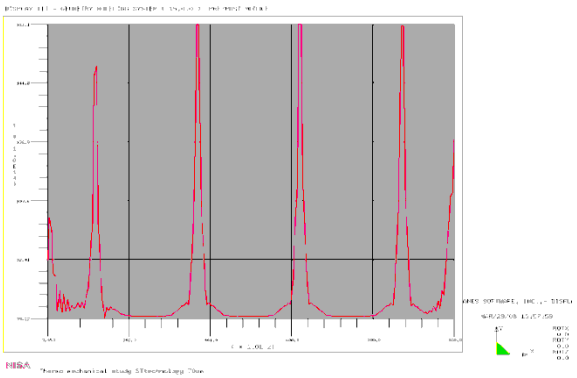


Figure 15: Sandwich forced convection through PCB surfaces simply supported in the bottom SHEAR STRESS through Y1-Bottom solders balls-WaferIC (70µm)

The maximum shear stress is of the order of **+16.1** MPa, acting on the bottom solders balls-WaferIC interface and the extreme variation is located on the solder ball interface. This is justified by the fact that the heat is accumulated in the waferIC substrate, therefore the maximum thermal variation is found at the solder ball interface. On the other hand, the induced thermal stress is combined with the intrinsic one due to the fabrication processes as well as to the stress due to the TSV holes. Therefore, cumulative damage is likely to occur at the critical interface regions. As such layers are very thin; any imperfection in structure may lead to cracking and subsequent shear-initiated delamination of the WaferIC structure. The nature of such interface materials must therefore be considered very carefully in WaferBoard™ design for intense planar activity applications.

VI. CONCLUSION

The WaferBoard™ rapid prototyping platform for electronic systems, based on WaferIC, a wafer scale circuit, shows great promise. Its use in an electronics manufacturing process flow will result in significant time and cost savings. Several challenges in the design and fabrication of the platform have been outlined.

Postprocessing from a microfabrication standpoint requires careful planning and characterization, as several tasks have to be accomplished sequentially. Amongst other achieved results, the developed DRIE process achieving a 15:1 aspect ratio will prove very instrumental to the fabrication of TSVs.

From a thermo-mechanical standpoint, the effects of heat and stress on the WaferBoard™ structure's behavior are of great significance to the development of the technology. Large values of stress, distortion and warpage can be induced by various steps during operation and during post processing the TSVs. The highest effective stress appears in the corners if the device is clamped and the maximum variation is found at solder ball interface.

Work is currently being done to make the postprocessing requirements less stringent. Larger via sizes in a thicker wafer are being considered for easier filling and greater strength, and a wider pitch is being envisaged to limit overall stress.

The integrated multidisciplinary design approach utilized so far will certainly help overcome most of these challenges.

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