Area and Power Optimization of High-Order Gain Calibration in Digitally-Enhanced Pipelined ADCs

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***Abstract*—Digital calibration techniques are widely utilized to linearize pipelined analog-to-digital converters (ADCs). However, their power dissipation can be prohibitively high, particularly when high-order gain calibration is needed. This paper demonstrates the need for high-order gain calibration in pipelined ADCs designed using low-gain opamps in scaled digital CMOS. For high-order gain calibration, this paper then proposes a design methodology to optimize the data precision (number of bits) within the digital calibration unit. Thus, the power dissipation and chip area of the calibration unit can be minimized, without affecting the ADC linearity. A 90-nm field-programmable gate array synthesis of a second-order gain calibration unit shows that the proposed optimization methodology results in 53% and 30% reductions in digital power dissipation and chip area, respectively.**

***Index Terms*—Analog-to-digital conversion (ADC), digital background calibration, pipeline.**

I. Introduction

THE PIPELINED analog-to-digital converter (ADC) is an attractive architecture for high-speed data conversion in CMOS technologies. However, its linearity is limited due to its reliance on precise analog component matching [1] and signal processing. Consider a typical pipeline stage with digital redundancy [2], as shown in Fig. 1. In its switched-capacitor circuit implementation, the primary source of linearity error is the gain error (due to opamp nonidealities and analog component matching) in its multiplying digital-to-analog converter (MDAC).

Digital calibration techniques can mitigate the linearity errors due to analog-circuit nonidealities in pipelined ADCs [3]–[8]. These techniques model the gain error in the MDAC of a pipeline stage as a zero-order (constant) error [3]–[5] or a second-order (nonlinear) error [6]–[8]. This error is then estimated and corrected for in the digital domain. For a given linearity, the dc-gain requirements on the MDAC opamp are more relaxed when using a second-order, rather than a zero-order, gain calibration technique (Section III). Hence, a higher order gain calibration technique is more suited for low-power analog design, particularly in nanometer digital CMOS processes. In these scaled processes, high dc gains for the opamps are difficult to achieve at low power, due to the low supply voltages and the poor intrinsic gains of the MOS transistors.

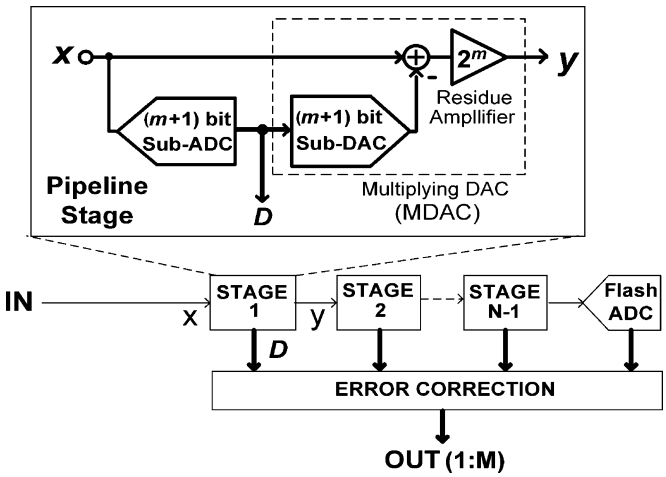

Fig. 1. M-bit N-stage pipelined ADC. Its first pipeline stage has an m-bit effective resolution and a 1-bit redundancy for digital error correction.

However, the digital circuit implementation of high-order gain-calibration techniques can require prohibitively-high power dissipation and chip area. This is because previously-reported algorithms for second-order gain calibration are computationally expensive to implement [9], requiring high-precision multipliers, adders, accumulators, and registers. This paper demonstrates how these algorithms can be simplified to render their digital circuit implementation more affordable in terms of both digital power and chip area.

Accordingly, this paper proposes a design methodology for minimizing both the power dissipation and chip area of the digital calibration unit, in pipelined ADCs with second-order background or foreground gain calibration. It first identifies the digital components in the circuit implementation of the calibration unit that dissipate a significant amount of power. It then demonstrates that, rather than using full data precision (number of bits) for all signals within these circuit components [9], the data precision of carefully-selected signals can be reduced to minimize the power dissipation and chip area of the digital calibration unit without affecting the linearity or resolution of the pipelined ADC.

To confirm the achievable savings in digital power dissipation and chip area using the proposed design methodology, the calibration unit of the pipelined ADC must be designed and implemented for various data precisions. Since custom silicon implementation of the calibration-unit design for each data precision

Manuscript received July 22, 2008; revised October 15, 2008. First published October 30, 2009; current version published March 24, 2010. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and by the Fonds Québécois de la Recherche sur la Nature & les Technologies.

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Digital Object Identifier 10.1109/TVLSI.2009.2014773

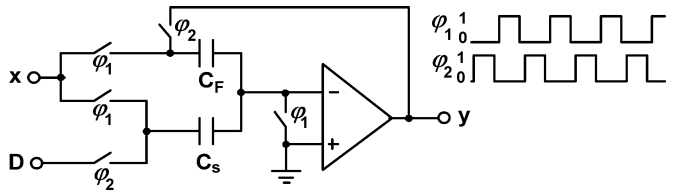


Fig. 2. Capacitor-flip-over MDAC for a 1-bit pipeline stage (Fig. 1).

is expensive, the calibration-unit designs for various data precisions are synthesized on a state-of-the-art 1.2-V 90-nm FPGA, and their power and area requirements are then computed and compared.

Section II reviews the gain calibration techniques for pipelined ADCs. Section III demonstrates the importance of high-order gain calibration for low-power design of high-resolution pipelined ADCs in nanometer digital CMOS. Section IV studies the computational complexity of second-order gain calibration. Section V describes the proposed design methodology for data-precision optimization in digital calibration units with second-order gain calibration. Section VI demonstrates the achievable savings in power and chip area.

II. Gain Calibration Techniques

Consider the "capacitor-flip-over" MDAC in Fig. 2, which is widely utilized to realize switched-capacitor pipeline stages with 1-bit effective resolution (Fig. 1). The MDAC output (the opamp output) signal can be expressed as

$$y = (1 - \delta g)(2x - DV_{\mathrm{REF}}) \tag{1}$$

where δg represents the overall gain error due to opamp nonidealities and capacitor mismatches [4]. Here, digit D (i.e., the sub-ADC output of the first pipeline stage in Fig. 1) is ± 1 or 0, depending on input signal x. In this paper, a unity reference voltage $(V_{\mathrm{REF}} = 1)$ is assumed for simplicity.

Gain error δg in (1) is not constant, but rather a nonlinear function of output signal y. Using a k^{th}-order Taylor series expansion, this gain error can be modeled as

$$\delta g = \delta g_0 + \delta g_2 y^2 + \delta g_4 y^4 + \cdots + \delta g_k y^k. \tag{2}$$

Here, a fully-differential MDAC is assumed, resulting in a zero value for the odd-order coefficients in the series expansion of δg.

A. Zero-Order Gain Calibration

To minimize computational complexity, most calibration techniques model gain error δg as a constant error [3], [4]

$$\delta g = \delta g_0. \tag{3}$$

Since, in the Taylor series expansion in (2), only errors due to δg_0 are then digitally calibrated, such techniques are classified as *zero-order* gain calibration techniques.

B. Second-Order Gain Calibration

To account for the inevitable nonlinear gain errors in the analog circuits, second-order gain calibration techniques have been proposed [6]–[8]. Here, gain error δg is modeled as a second-order nonlinear function of output signal y

$$\delta g = \delta g_0 + \delta g_2 y^2. \tag{4}$$

Gain errors due to δg_0 and δg_2 are then digitally calibrated.

III. Importance of High-Order Gain Calibration

A. Gain Errors Due to the Nonlinear DC Gains of Opamps

In a CMOS opamp, the dc gain varies with the output voltage, due to the dependence of the output resistance of an MOS transistor on its drain–source voltage. This nonlinear variation in the opamp dc gain A can be modeled as a function of the opamp output voltage y using, [10], [11]

$$A = \begin{cases} A_0\left(1 - (y/y_{\mathrm{sat}})^2\right), & \text{for} \quad y < y_{\mathrm{sat}} \\ 0, & \text{for} \quad y \geq y_{\mathrm{sat}} \end{cases} \tag{5}$$

where A_0 is the maximum dc gain and y_{sat} is the output saturation voltage of the opamp [10], [11]. Hence, using a Taylor series expansion, the inverse of the opamp dc gain can be expressed for $y < y_{\mathrm{sat}}$ as

$$\frac{1}{A} = \frac{1}{A_0}\left(1 + \left(\frac{y}{y_{\mathrm{sat}}}\right)^2 + \left(\frac{y}{y_{\mathrm{sat}}}\right)^4 + \cdots\right). \tag{6}$$

Assume that the gain error δg in a switched-capacitor MDAC is only due to the finite dc gain of its opamp. Based on negative feedback theory, the value of δg can then be expressed as [12]

$$\delta g = \frac{1}{1 + A\beta} \approx \frac{1}{A\beta} \tag{7}$$

where β is the feedback factor of the MDAC during its charge-transfer clock phase [12]. Hence, (6) and (7) lead to

$$\delta g = \frac{1}{A_0\beta}\left(1 + \left(\frac{y}{y_{\mathrm{sat}}}\right)^2 + \left(\frac{y}{y_{\mathrm{sat}}}\right)^4 + \cdots\right). \tag{8}$$

Therefore, δg increases with decreasing A_0. Furthermore, the effect of the k^{th}-order error term on δg increases with $(y_{\mathrm{sat}})^{-k}$. Accordingly in nanometer digital CMOS technologies, the high-order error terms have a significant contribution to the total gain error δg due to the following: 1) the low supply voltages (and, hence, the low saturation voltage y_{sat} of the opamp) and 2) the low intrinsic gains of the MOS transistors (and, hence, the low dc gain A_0 of the opamp) in these scaled technologies.

B. Importance of Second-Order Gain Calibration

To study the importance of high-order gain calibration, a zero-order [4] and a second-order [7] gain calibration technique are implemented in a 14-bit pipelined ADC. The pipeline core

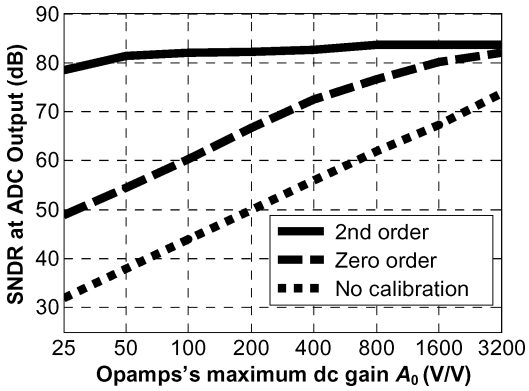


Fig. 3. SNDR versus opamp's maximum dc gain A_0, with no calibration, zero-order gain calibration [4], and second-order gain calibration [7].

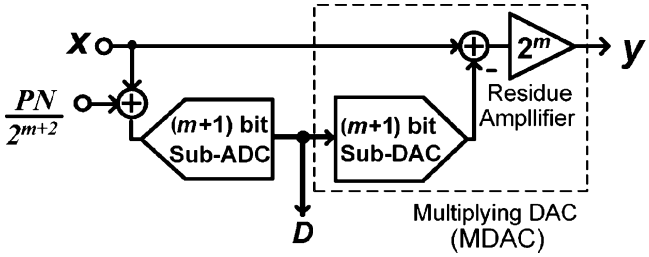


Fig. 4. First pipeline stage (with m-bit effective resolution) of the M-bit pipelined ADC in Fig. 1, with a dither signal PN added at the input of its sub-ADC.

of this ADC is partitioned into fourteen 1.5-bit stages. Behavioral simulations of the ADC are performed in SIMULINK, with the switched-capacitor amplifiers in the MDACs modeled as described in [12]. Only the first pipeline stage is assumed to be nonideal, as the ADC performance is most sensitive to nonidealities in its front-end stage. The error due to the nonlinear dc gain of the opamp in the first pipeline stage is modeled as described in (5). No other error sources are included. Here, $V_{\rm REF} = 1$ V and $y_{\rm sat} = 1.414V_{\rm REF}$ are assumed. A 0.9-V sinusoid is applied at the ADC input.

Fig. 3 shows the SNDR at the ADC output versus opamp's maximum dc gain A_0, with: no calibration, zero-order gain calibration [4], and second-order gain calibration [7]. Accordingly, for over 74-dB (12-bits) SNDR, opamps with dc gains of 71 dB (3500 V/V), 56 dB (630 V/V), and 26 dB (20 V/V) are required when using no calibration, zero-order gain calibration, and second-order gain calibration, respectively. Therefore, second-order gain-calibration techniques significantly relax (by 30 dB) the requirements on the opamp dc gains.

Accordingly, high-order gain calibration techniques are critical for designing high-resolution high-speed pipelined ADCs in nanometer digital CMOS technologies using moderate-gain opamps and, hence, at low power dissipation. In these scaled technologies, opamps with high dc gains require either multiple gain stages or output-impedance enhancement, because of the shrinking supply voltages and the poor intrinsic gains of the MOS transistors. Such gain-boosting techniques for the opamps can significantly increase the power dissipation and degrade the speed.

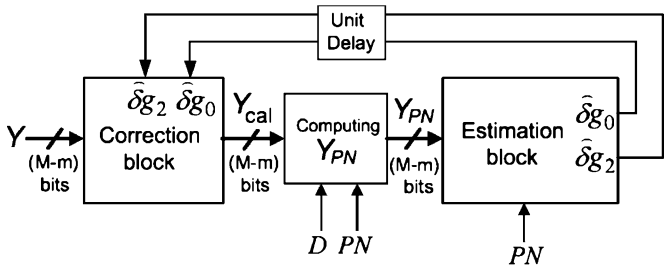


Fig. 5. Digital calibration unit for the second-order gain calibration of the pipeline stage in Fig. 4.

Note that the linearity errors due to opamp dynamics (slew rate and bandwidth) [12] were not accounted for in the behavioral simulations shown in Fig. 3. The degrading effect of these opamp nonidealities on the SNDR is much more significant when only zero-order calibration is used. This further stresses the need for second-order gain calibration techniques in high-resolution pipelined ADCs.

In the following, the second-order gain calibration algorithm in [7] is summarized to illustrate the computational complexity of second-order gain-calibration techniques.

IV. Computational Complexity of Second-Order Gain Calibration

Consider the first pipeline stage (with m-bit effective resolution) in the M-bit pipelined ADC of Fig. 1. To calibrate gain error δg in its MDAC output y in (1), a known dither signal PN (i.e., a pseudorandom sequence PN) is added at the input of its sub-ADC, as shown in Fig. 4 [4], [7].

Assume that the first pipeline stage (Fig. 4) has a 1-bit effective resolution $(m = 1)$.

Let Y denote the digital representation of output signal y in the first pipeline stage, as digitized by the subsequent pipeline stages (Fig. 1). Furthermore, let $Y_{\rm cal}$ denote the calibrated value of Y. Then, after calibrating its first pipeline stage, the calibrated value of the M-bit output word OUT of the pipelined ADC (Fig. 1) can be expressed as

$$OUT_{\rm cal} = \frac{1}{2}(D + Y_{\rm cal}) \tag{9}$$

where D is the digital output of the sub-ADC in the first pipeline stage (Fig. 4).

Fig. 5 shows the building blocks of the digital calibration unit, which can be used for the second-order gain calibration of the pipeline stage in Fig. 4. Every clock cycle, this second-order digital calibration unit (Fig. 5) performs the following tasks.

1) *Correction block*: Output Y is corrected based on the estimated values for δg_0 and δg_2, thus generating $Y_{\rm cal}$.
2) *Computing* Y_{PN}: An intermediate digital signal

$$Y_{PN} \equiv 2OUT_{\rm cal} - \left(D - \frac{PN}{2}\right) = Y_{\rm cal} + \frac{PN}{2} \tag{10}$$

is computed.
3) *Estimation block*: The estimated values of δg_0 and δg_2 are updated, based on the linearity errors in signal Y_{PN}.

The correction and estimation blocks are described in the following.

A. Correction Block

The output signal y of the first pipeline stage is digitized as Y by the subsequent pipeline stages (Fig. 1). Thus, Y is available in the digital domain. To digitally correct for gain error δg, the correction block of the calibration unit (Fig. 5) multiplies the digitized output signal Y by $(1+\widehat{\delta}g)$, where $\widehat{\delta}g$ is the estimated value of gain error δg. For second-order gain calibration, the correction algorithm is

$$\widehat{\delta}g = \widehat{\delta}g_0 + \widehat{\delta}g_2 Y^2 \tag{11}$$

$$Y_{\text{cal}} = Y \cdot (1+\widehat{\delta}g) \tag{12}$$

where Y_{cal} is the corrected (calibrated) value of Y, while $\widehat{\delta}g_0$ and $\widehat{\delta}g_2$ are the estimated values for the zero- and second-order gain error terms δg_0 and δg_2, respectively.

B. Estimation Block

For second-order gain calibration, the values of the gain error terms δg_0 and δg_2 must be digitally estimated. To illustrate the complexity associated with second-order gain error estimation, consider the iterative relations presented[1] in [7] to estimate δg_0 and δg_2

$$\widehat{\delta}g_0(n+1) = \widehat{\delta}g_0(n) + \mu_0 \cdot PN \cdot Y_{PN} \tag{13}$$

$$\widehat{\delta}g_2(n+1) = \widehat{\delta}g_2(n) + \mu_2 \cdot \left(E\left[PN \cdot Y_{PN}^3\right] - 3 \cdot E[PN \cdot Y_{PN}] \cdot E\left[Y_{PN}^2\right]\right). \tag{14}$$

Here, n is the iteration index, μ_0 and μ_2 are the update step sizes, and $E[.]$ denotes the average over a large number of samples. It is shown[1] in [7] that iterative relations (13) and (14) converge to the actual values of δg_0 and δg_2.

C. Digital Circuit Complexity

To estimate the values of δg_0 and δg_2 for second-order gain calibration, the iterative relations in (13) and (14) must be digitally implemented. To simplify the digital circuit implementation of the multiplications by μ_0 and μ_2 in these relations, the values of μ_0 and μ_2 are typically selected as 2^{-k0} and 2^{-k2}, where $k0$ and $k2$ are integer constants. Thus, these multiplications can be performed by $k0$ and $k2$ shifts in the multiplicand. Furthermore, since the pseudorandom signal PN is either $+1$ or -1, the multiplication by PN in (13) and (14) can also be performed by changing the sign of the multiplicand. Moreover, the averaging operation $E[.]$ can be performed using an accumulator.

However, digital multipliers are still required to compute Y_{PN}^2, Y_{PN}^3, and $E[Y_{PN}^2] \cdot E[PN \cdot Y_{PN}^3]$ in iterative relation (14) for the second-order error term $\widehat{\delta}g_2$. These digital multiplications are expensive to implement in terms of digital power and area.

In the following, a design methodology is proposed to significantly reduce the circuit implementation complexity of the multiplications and accumulations in iterative relations (13) and (14). Thus the power dissipation and chip area required for the digital circuit implementation of second-order gain-calibration techniques can be minimized, without affecting the linearity of pipelined ADCs.

[1]Our goal here is to only illustrate the digital complexity of second-order gain-error estimation in order to later demonstrate (in Section V) how this digital complexity and, hence, the required power dissipation and chip area can be significantly reduced. The reader is referred to [7] for detailed derivations of relations (13) and (14).

V. Design Methodology for Power Optimization

A. Data Precision of Y_{PN}

In the estimation block of a second-order gain calibration unit (Fig. 5), the complexity of the digital multipliers and accumulators—used to implement iterative relations (13) and (14)—mostly depends on the data precision (number of bits) of digital signal Y_{PN}. In an M-bit pipelined ADC (Fig. 1), the full precision of Y_{PN} is $(M-m)$ bits, assuming an m-bit effective resolution in the first pipeline stage. Reducing the data precision of Y_{PN} reduces the computational complexity and, hence, the power and area for the digital circuits.

Reducing the precision of Y_{PN} by truncating some of its least significant bits (LSBs) is equivalent to adding some quantization noise to Y_{PN}. Assuming that this quantization noise is uncorrelated with signal Y_{PN} and pseudorandom sequence PN, it will be filtered out by the accumulators used to implement iterative relations (13) and (14) [4]. Therefore, a truncated Y_{PN} (i.e., a Y_{PN} with some of its LSBs removed) can be utilized in the estimation block instead of Y_{PN}.

However, there is a weak correlation between Y_{PN} and the quantization noise associated with a truncated Y_{PN} [4]. This affects the convergence of iterative relations (13) and (14). Depending on the amount of quantization noise and its correlation with the ADC input signal, the accuracy of the gain calibration and, hence, the total ADC resolution can degrade. This limits the maximum number of LSBs that can be truncated from Y_{PN}, without affecting the accuracy of the gain calibration. Due to the complex behavior of the quantization noise in the calibration unit and its correlation with the ADC input signal, no mathematical expressions are derived for the optimal data precision. Rather, in Section VI, the optimal data precision (number of bits) for Y_{PN} will be determined through system-level simulations.

The power and area optimization technique proposed earlier for the estimation block in second-order gain calibration can also be utilized in zero-order gain calibration, since both zero-order [3], [4] and second-order [7] calibration methods essentially use relation (13) to estimate the zero-order gain error term δg_0 in their respective estimation blocks.

B. Data Precision of Y

In an M-bit pipelined ADC (Fig. 1), the full precision of Y is $(M-m)$ bits, assuming an m-bit effective resolution in its first pipeline stage. The value of Y used to compute Y_{cal} in (12) and, subsequently, OUT_{cal} in (9) should always be implemented at its full precision, since its precision directly impacts the accuracy at the output of the pipelined ADC.

However, the accuracy of the estimated gain error $\widehat{\delta}g$ used in the correction block of a second-order gain-calibration unit (Fig. 5) is determined by the accuracy of $\widehat{\delta}g_0$, $\widehat{\delta}g_2$, and Y_2 as per

relation (11). Since $\widehat{\delta g}_0$ and $\widehat{\delta g}_2$ are the outputs of two accumulators, their values change moderately around their mean values, owing to the randomness of the accumulated signal. Therefore, having an accurate Y^2 does not significantly improve the accuracy of the estimated $\widehat{\delta g}$ since its other components (i.e., $\widehat{\delta g}_0$ and $\widehat{\delta g}_2$) in (11) are not very accurately estimated. Hence, the data precision (number of bits) of Y can also be reduced when computing $\widehat{\delta g}$, without affecting the accuracy of the gain calibration. In Section VI, the optimum data precision for Y will be determined through system-level simulations.

The power and area optimization technique proposed here for the correction block in background digital calibration can also be utilized in foreground digital calibration, since both background [3]–[7] and foreground [8] calibration methods use similar correction blocks.

VI. FPGA Synthesis Results

To estimate the achievable savings in digital power dissipation and chip area, the second-order gain calibration algorithm in [7] is synthesized on an FPGA (EP2C5T144C6, Cyclone II, 90 nm, 1.2 V) before and after using the proposed design methodology for power and area optimization. To measure the achievable linearity for the pipelined ADC, behavioral simulations of the ADC and its digital calibration unit are then performed in SIMULINK [12].

The pipelined ADC is partitioned into 14 pipeline stages, each with a 1-bit effective resolution. In the SIMULINK behavioral simulations, the input–output transfer function of the MDAC in each pipeline stage is modeled as in (1), with a gain error δg. Only the MDAC in the first pipeline stage is assumed to have gain errors. Furthermore, only gain errors due to the nonlinear dc gain of its opamp are modeled as per (5), assuming a maximum dc gain $A_0 = 100$ V/V and an output saturation voltage $y_{\rm sat} = 1.414$ V. Hence, considering only a second-order expression for gain error δg as in (4), this results in

$$\delta g = 0.02 + 0.01y^2 \tag{15}$$

for a 1.5-bit MDAC with a feedback factor $\beta = 0.5$ (i.e., neglecting any capacitor mismatch or parasitic capacitors). A 0.9-V sinusoidal signal is applied at the ADC input.

The values of step sizes μ_o and μ_2 in iterative relations (13) and (14) are set to 2^{-22} and 2^{-14}, respectively. On the FPGA, the averaging in (14) is realized using low-pass filters. Each low-pass filter is implemented using an accumulator as

$$E[x](n+1) = E[x](n) + \mu_e \cdot (x - E[x](n)) \tag{16}$$

where n is the iteration index and $\mu_e = 2^{-19}$.

The second-order digital calibration unit (Fig. 5) is synthesized on the FPGA, and its *dynamic* power dissipation is estimated using Quartus II. The clock frequency of the FPGA is set at 100 MHz. A random signal Y is applied at the input of the calibration unit (Fig. 5) to estimate its worst-case *dynamic* power dissipation. To estimate its *static* power dissipation, an estimate of the ratio of the calibration-unit area to the total FPGA area is calculated and then multiplied by the total static power dissipation of the FPGA (which is available in its data sheet).

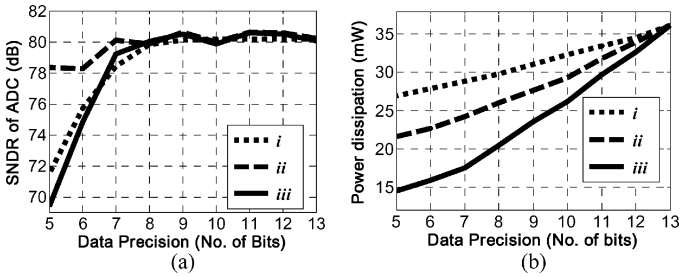


Fig. 6. (a) SNDR of the calibrated pipelined ADC based on MATLAB simulations and (b) the power dissipation of its digital calibration unit (Fig. 5) based on FPGA synthesis versus the following: ***i***) number of bits in Y, with Y_{PN} having its full precision (13 bits); ***ii***) number of bits in Y_{PN} having its full precision (13 bits); and ***iii***) number of bits in Y_{PN} and Y.

Fig. 6 shows the SNDR at the ADC output and the power dissipation in its digital calibration unit versus the following:

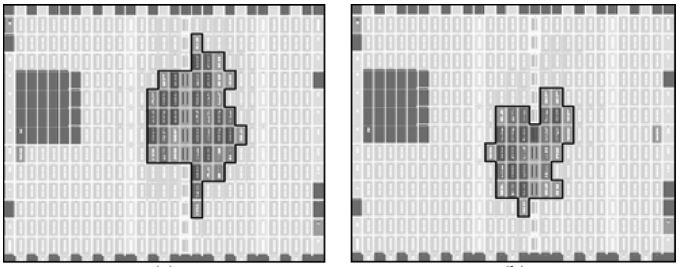
i) data precision of Y, with Y_{PN} having full 13-bit precision;
ii) data precision of Y_{PN}, with Y having full 13-bit precision;
iii) data precisions of Y and Y_{PN}.

Based on Fig. 6(a), the data precisions of Y and Y_{PN} can be reduced from full 13 to 7 bits while still achieving an $\mathrm{SNDR} > 79$ dB (13 bits). Based on Fig. 6(b), such data-precision reduction in Y and Y_{PN} (from full 13 to 7 bits) saves 53% of the total power dissipation in the calibration unit.

If the second pipeline stage (STAGE 2) of the M-bit pipelined ADC (with N stages in Fig. 1) also requires calibration, then the proposed optimization technique can be equally applied to the digital-calibration unit of STAGE 2, assuming that STAGE 2 is the first pipeline stage of a pipelined ADC formed by STAGE 2 to STAGE N with $(M - m)$ bits of resolution (where m is the resolution of STAGE 1 in Fig. 1). For example, in the pipelined ADC under consideration (with $M = 14$ bits and $m = 1$ bits), this is equivalent to calibrating the first pipeline stage of a 13-bits $(\mathrm{SNDR} > 74$ dB$)$ pipelined ADC. Accordingly, assuming that the gain error δg of STAGE 2 is given in (15), then based on Fig. 6(a), the precisions of Y and Y_{PN} in the calibration unit for STAGE 2 can be reduced from their full 12 to 6 bit resolution. Furthermore, based on Fig. 6(b), such data-precision reduction in Y and Y_{PN} (from full 12 to 6 bits) saves 52% of the total power dissipation in the digital calibration unit of STAGE 2. Note that, during the calibration of the first pipeline stage using the digital background calibration techniques in [4] and [7], the second pipeline stage is assumed to be either ideal or calibrated. Therefore, the calibration of the second pipeline stage must be performed either before or concurrently with the first pipeline stage.

Note that the reported power-dissipation values are extracted using an automated compilation of the VHDL code for the gain calibration algorithm. With custom silicon design of the digital calibration unit, this power dissipation can be further reduced [9], making high-order gain calibration techniques even more practical in high-resolution ADCs.

Fig. 7 compares the size of the digital calibration unit when synthesized on the FPGA, using the full 13-bit data precision and the reduced 7-bit data precision. Thus, reducing the data



(a) (b)

Fig. 7. Area of the calibration unit on the FPGA when synthesized with: (a) full data precision (13 bits) for Y and Y_{PN} and (b) precision of Y and Y_{PN} reduced from full 13 to 7 bits.

precision from full 13 to 7 bits saves 30% of the area of the calibration unit (Fig. 7) without affecting the SNDR at the output of the ADC as shown in Fig. 6(a).

VII. Conclusion

High-order gain calibration is required to achieve high resolution in pipelined ADCs designed using low-gain opamps in low-voltage scaled digital CMOS technologies. A design methodology was proposed to optimize the data precision within the ADC calibration unit, thus minimizing the power dissipation and chip area without affecting the ADC resolution and linearity. The proposed design methodology has been demonstrated to significantly reduce the area and power dissipation of the digital calibration unit in pipelined ADCs with second-order gain calibration.

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