Electrical characterization of annular Through Silicon Vias for a Reconfigurable Wafer-sized Circuit Board

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***Abstract*— This paper presents the electrical characterization of annular TSV technology for full wafer applications. A possible utilization of this technology is the WaferBoard™, a reconfigurable circuit board for rapid system prototyping. Electrical resistance and capacitance of a single 2-4µm thick annular TSV with a diameter of 110µm and a height of 350µm are measured to be about 10mΩ and 0.27pF, respectively. TSV yield of 98% is reached over the wafer. Results also show electrical failure of some TSVs due to poor via filling.**

Keywords-component:* WaferBoard™, *annular TSV, electrical resistance and capacitance.

I. INTRODUCTION

The last several decades have seen an extraordinary increase in the functionality of electronic systems mainly driven by the scaling of semiconductor devices. However, this upward trend meets serious constrains related to lithographic scaling limits and inability of power densities to allow reliable system to be fabricated. Therefore, it becomes a big challenge to increase system performance. One of the most serious candidates is three dimensional (3D) integration technology which allows better electrical performance, higher interconnects density and, wider heterogeneous systems integration [1]. The main challenge in 3D technology relates to vertical interconnections; schemes such as flip chip, wire bonding, and through silicon vias (TSVs) constitute vertical interconnection alternatives. Among these 3D interconnects, TSV technology is currently considered one of the most promising concepts that could address the limitations of today's packaging technology [2].

The work reported on TSVs during the last decade exhibits a wide variety of approaches for the choice of aspect ratios, dielectric thicknesses, fill materials, and potential applications [2-6]. For the most part, a full filled cylindrical via geometry is used in TSV technology. In the recent years, the annular via geometry has been the focus for industry research institutes and has been demonstrated to have lower electrical resistance and better thermal stability. In fact, annular TSVs typically have a resistance lower than 20mΩ [7], while fully filled TSV resistance values vary from 20 mΩ to 350Ω [2-5]. Lu et al. have reported that the residual thermal stresses around TSVs induced by the TSV manufacturing processes can be significantly reduced by changing the via geometry from cylindrical to annular [8]. However, the TSV concept based on the annular geometry still requires further studying especially on the investigation of reliability issues. Furthermore, annular via technology must be extended to full wafer applications in order to achieve reduced manufacturing cost and highly integrated systems.

In this paper, we present the analysis of electrical reliability of annular TSVs implemented in a full wafer (200mm). An example of full wafer integration using annular TSVs described in this paper is a reconfigurable circuit board for a rapid electronic systems prototyping platform called WaferBoard™ [9]. The first section briefly reviews the concept of WaferBoard™ with emphasis on the role of TVSs in this application. Then, the second section presents a description of the TSV chains and their manufacturing process flow. Finally, the last section reports single TSV resistance and capacitance measurements and electrical continuity of TSV chains as well as TSV yield throughout the wafer.

II. WAFERBOARD™ OVERVIEW

At the prototyping stage several iterations of a complex interconnection network often need to be implemented. Each requiring the tedious and time consuming redesign of a Printed Circuit Board (PCB). To meet the tight constraints on size, power efficiency and time-to-market, new techniques for prototyping of electronic systems need to be put in place. WaferBoard™, a rapid prototyping technology based on a wafer-sized circuit, WaferIC™ [9], is proposed to mitigate this development and prototyping bottleneck.

The WaferIC™, as illustrated in Fig. 1, consists of several stacked layers. At the top of the stack, an anisotropic conductive film (ACF) formed with high density micro metallic fibers, is deposited on an array of more than one million tiny (90µmx90µm) conducting pads (NanoPads™). NanoPads™ array coats a mature 7-metal layer CMOS 0.18µm technology that contains an internal programmable interconnect network. An array of annular TSVs connects the CMOS layers to the bottom layer of the WaferIC™, which is the power supply mechanism containing circuitry such as a point-of load voltage converters and decoupling capacitors to regulate the WaferIC™ supply. To prototype electronic systems, components that are packaged in Ball Grid Array (BGA), Quad Flat Package (QFP), etc. or user ICs (uICs) can simply be placed anywhere on the WaferIC™ surface, which is alignment-insensitive. This smart surface detects and maps the uICs contacts, and builds the electrical connections between them. These connections are programmed during a

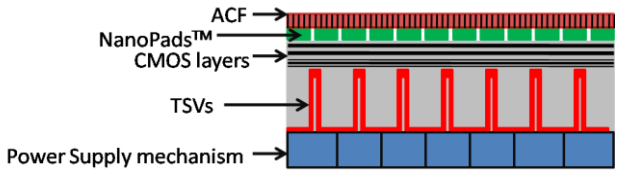

Figure 1. Schematic of WaferIC™ stack.

configuration step, similar to FPGA (field-programmable gate array). To achieve this goal, annular TSVs are used to feed the WaferIC™ from underneath directly into an internal WaferIC™ power distribution grid that starts on metal 1 (M1), TSVs also provide JTAG signals to configure or to program the WaferIC™ internal circuitry prior to operation.

III. PRESENTATION OF THE DEVELOPMENT WAFER

To electrically characterize the annular TSVs chosen for the WaferBoard™ application, a 200mm post-processing full wafer named development wafer is manufactured. The development wafer holds many different test structures, and a single CMOS metal layer, M1, no active devices are present. In addition, the wafer contains 76 repetitive wafer fields (square of 17.92mmx17.92mm), each integrating a chain of 64 TSVs connected together by Al topside and Cu backside routing lines (Fig.2). On the wafer topside, a 3-5µm thick Cu layer is deposited onto a 0.54µm thick Al layer forming a pad on each TSV. The resulting stack is named TSV landing pad (Fig.2(a)) and it is used for vias probing for electrical tests (section IV).

Before addressing the characterization of TSVs, one must focus on the TSV process flow. The manufacturing of the TSVarray begins with deep reactive ion etching (DRIE) for creation of a via or hole through the processed silicon wafer. Etching stops at the oxide underneath the M1 layer. This is followed by a coating of a sidewall with oxide (Tetra-Ethyl-Ortho-Silicate or TEOS source gas) preventing electrical leakage. Then, in order to reach M1, a dry etching of the oxide underneath this metal layer is curried out. After this, the vias are filled with copper electroplated on a seed layer to achieve low interconnection resistance between M1 and the silicon backside. In this case, the vias are not completely filled. Instead, it forms a 2-4µm thick annular copper layer around the edges of the vias. This copper is then used to create a

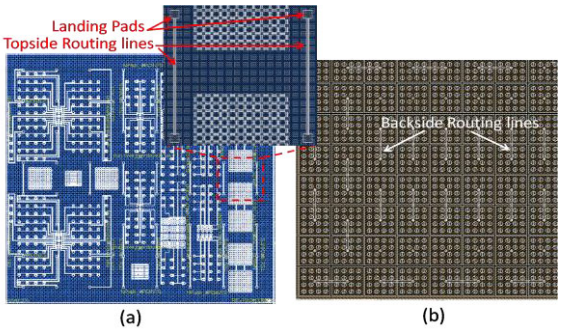

Figure 2. One wafer field design (a) Topside and (b) Backside.

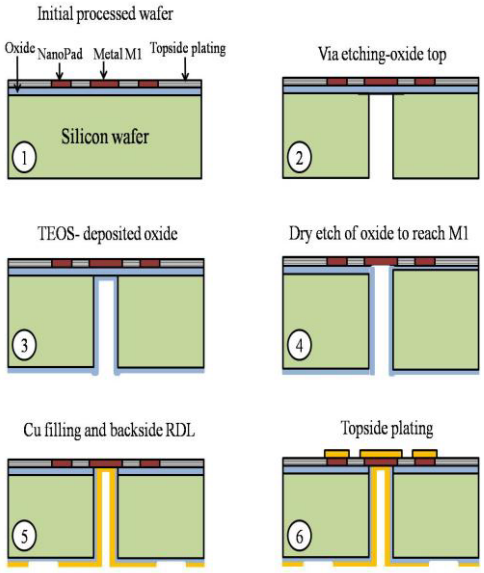

Figure 3. TSV process flow.

backside redistribution layer (RDL). Finally, plating is accomplished at the top of the wafer to produce thick protruding NanoPads™ and TSV landing pads used for electrical probing. Chemical mechanical planarization (CMP) steps are also performed as needed for the planarity of layers. The process flow is outlined in Fig. 3. A via array with an average diameter of 110µm has been successfully completed throughout a 350µm thick wafer.

IV. ELECTRICAL RESULTS AND DISCUSSIONS

A. *Single TSV electrical Characterization*

The electrical parameters of annular TSVs measured in this work are the resistance and the capacitance. For the resistance of the TSVs, measurements were performed using two methods both utilizing a four-probing technique. With the first one, a chain of two TSVs connected by a Cu backside routing line was tested. This 2-TSV chain is illustrated in Fig. 4(a) and shows that current enters in the first TSV (TSV_1) then flows through the Cu backside line and leaves through the second TSV (TSV_2). One can easily deduce from Fig. 4(a) the equivalent circuit model shown in Fig. 4(b) and extract the equivalent resistance $R_{equivalent}$ as the sum of the TSVs resistance $2*R_{TSV}$ and the resistance of Cu backside line $R_{Cu-Line}$:

$$R_{equivalent}=2*R_{TSV}+R_{Cu-Line} \quad (1)$$

Several tests are performed on different sites of the development wafer to determine $R_{equivalent}$. The average value of $R_{equivalent}$ is 31.8mΩ. $R_{Cu-Line}$ was previously measured by directly probing the wafer backside and its value is equal to 10.9mΩ. Plugging these values into (1), one obtains the resistance of a single TSV of 10.45mΩ.

The second method presented in Fig.4(c) is based on the

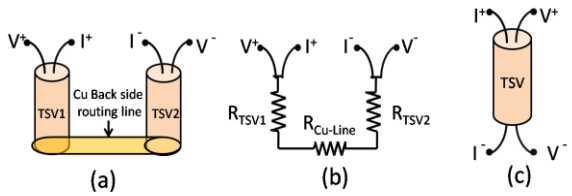

Figure 4. Schematics of resistance measurement (a) the 2-TSV chain test, (b) the equivalent circuit model of (a) and (c) the direct test of single TSV.

direct measurement of the resistance of one TSV using direct probing of the topside TSV landing pad and the backside TSV pad. The resistance values of several TSVs are plotted in Fig.5. R_{TSV} values vary from 8.9mΩ to 11.4 mΩ and the average resistance is equal to 10.5mΩ±0.6mΩ. The variation in resistance values is due to Cu filling thickness variation during TSV processing. The two methods give resistance values in good agreement.

Parasitic capacitance is also measured and in this case, the sidewall dielectric material and thickness are the critical parameters. The capacitance must be low enough to avoid signal delay increase. In our case, the parasitic capacitance measurements have been performed between the annular Cu inside the TSV, and the Si bulk around the TSV. For different TVSs, a capacitance value of 0.27pF±0.02pF has been found at frequency of 100kHz. This value is in the range of fully filled TSVs whose capacitance varies from 2fF to over 1pF, reported in [10]-[12].

The single annular TSV resistance and capacitance measured are very encouraging in validating the use of annular TSVs in full wafer applications. However, results need to be completed with via chain testing and TSV yield analysis throughout the wafer.

B. *Electrical continuity of TSVchains and TSV yield at wafer level*

The schematic of the TSVs chain is presented in Fig.6. First, the electrical continuity of TSV chains was tested by measuring their resistance between points A and B. Then, this testing chain allows determining the TSV yield at the wafer level.

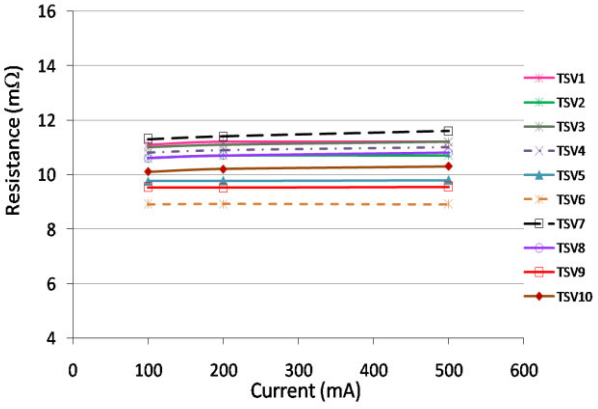

Figure 5. Resistance measurement of different annular TSVs.

The 76 TSV chains were tested and each measured resistance is called chain resistance for the sake of simplicity.

Different current values of 0.1mA, 1mA and 10mA are used as inputs parameters and a voltage limit of 40V is fixed. Fig. 7 presents the results obtained from this set of parameters and it shows chain resistance mapping throughout the wafer. 82.9% of TSV chains have resistances ranging from 202Ω to 234Ω while one chain has resistance 313Ω and 15.8% of chains (red regions) show values of tens of kilo ohms. These values were compared to the estimated chain resistance in order to determine whether the electrical continuity of the chains is good or not. The estimated chain resistance, R_{Chain}, can be divided into three components: (i) the resistance of the total topside routing lines $R_{Topside\text{-}Lines}$, (ii) the resistance of 48 vias R_{TSVs}, and (iii) the resistance of total backside routing lines $R_{Backside\text{-}Lines}$:

$$R_{Chain} = R_{Topside\text{-}Lines} + R_{TSVs} + R_{Backside\text{-}Line} \quad (2)$$

R_{TSVs} is obtained as 504mΩ (10.5mΩ multiplied by 48 vias) and the $R_{Topside\text{-}Lines}$, *and* $R_{Backside\text{-}Lines}$ are approximated by using the analytical formula for resistance R of a conductor of material resistivity of ρ, length l and uniform cross section S:

$$R = \rho l / S \quad (3)$$

Applying the above expression to the Al topside routing lines and the Cu backside routing lines gives values of 172.6Ω and 96m Ω for $R_{Topside\text{-}Lines}$ and $R_{Backside\text{-}Lines}$, respectively. Hence, R_{TSVs} and $R_{Backside\text{-}Lines}$ can be considered negligible in comparison to $R_{Topside\text{-}Lines}$, hence the value of R_{Chain} is mainly due to the topside routing. The estimated value of R_{Chain} allows us to state that 84% of chains demonstrate good electrical continuity. The difference between the corresponding measured chain resistances and the R_{Chain} estimate can be attributed to the approximation of geometrical uniformity made when using (3). The dispersion of the chain resistance values can be attributed to inhomogeneous thicknesses of the topside routing lines. Furthermore, the red regions can be considered electrically failed; focus is placed on these areas to determine the TSV yield as well as the origin of failure.

By testing different TSV series on each failed chain, one can to isolate the defective TSVs. For these TSVs, high resistances ranging from 1Ω to 12kΩ are measured. From these results, a TSV yield of 98% has been reached over the wafer.

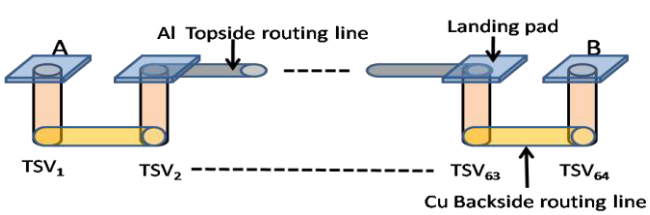

Figure 6. Schematic of TSV chain.

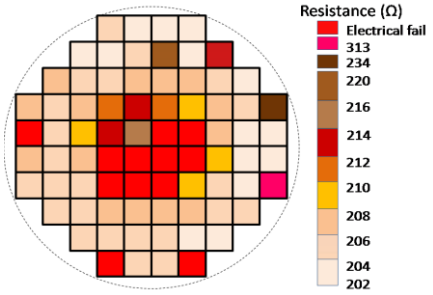

Figure 7. Chain resistance mapping of 76 wafer fields.

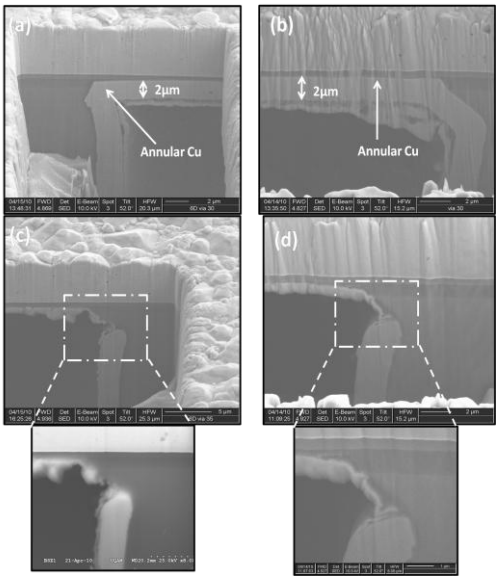

Figure 8. Dual Beam FIB/SEM images inside TSVs (a), (b), (c) and (d) have TSV resistance of 11mΩ, 10mΩ, 6kΩ, and 1.4kΩ, respectively.

To understand the origin of resistance failure, a dual beam FIB/SEM characterization was performed to compare defective TSVs with high resistances and TSVs with low resistances. Some of the characterization results are presented in Fig.8. TSVs shown exhibit resistances of 11mΩ, 10mΩ, 6kΩ and 1.4kΩ. From the figures, it is clear that the high TSV resistance is due to a poor Cu filling inside the via (Fig.8(c) and Fig.8(d)), while when a uniform 2µm Cu layer fills the TSV (Fig.8(a) and Fig.8(b)), a low resistance value is obtained. One also notices that almost all the defective vias are concentrated at the center of the wafer, leading to the hypothesis that Cu electroplating process suboptimal. Thus, this bad result is believed to be caused by the variations in local current density at the center of the 200mm wafer compared to its edges where the contact plating fixtures are positioned during the electroplating process. Another cause of the poor plating at the wafer center could be related to the control of fluid agitation, especially at the wafer surface where it directly impacts the hydrodynamic boundary layer thickness.

V. CONCLUSION

A TSV interconnect technology based on an annular geometry for full wafer applications is described with emphasis on the WaferBoard™, an innovative platform for rapid prototyping of electronic systems. TSV structures implemented in a development wafer were electrically characterized. Results indicated low resistance and parasitic capacitance values at single via level. These results, along with the high electrical via yield, show great promise for the full wafer applications. Some defective vias are noticed due to poor Cu deposition. The concentration of the defective vias on the center of the wafer suggests the necessity to optimize the electroplating process in order to achieve better Cu filling uniformity. Further work shall also include thermal management of annular TSVs.

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