A 1-V Process-Insensitive Current-Scalable Two-Stage Opamp With Enhanced DC Gain and Settling Behavior in 65-nm Digital CMOS

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***Abstract*—A pseudo-cascode compensation technique is proposed to enable a process-insensitive and current-scalable design of the classical two-stage opamp at low supply voltages, without requiring any additional power dissipation. Furthermore, a bulk-biasing technique is proposed to enhance the dc gain of the two-stage opamp, without affecting its output-voltage swing and without requiring any additional power dissipation. To compare the performance advantages of the proposed pseudo-cascode compensation technique versus classical Miller compensation in a two-stage opamp with/without applying the proposed bulk-biasing technique, four opamps were fabricated on the same die in a 1-V 65-nm CMOS process. The corresponding transistors in all four opamps had equal sizes. Furthermore, all four opamps had equal total compensation capacitance and the same total power dissipation. Accordingly, compared to using Miller compensation, by applying the proposed pseudo-cascode-compensation and bulk-biasing techniques in a two-stage opamp, the opamp's dc gain is increased by a factor of 4 (12 dB), its unit-gain frequency is increased by 40%, and its phase margin is maintained over a factor of 100 scaling in its bias current. Furthermore, the overshoot in its large-signal step response is eliminated and the rise/fall settling times are improved by 33%. The trade-off is a minimal decrease in the opamp's phase margin. Importantly, this is all achieved without affecting the opamp's output-voltage swing and without requiring any additional power dissipation.**

***Index Terms*—Frequency compensation, gain enhancement, low power, low voltage, operational amplifier, process insensitive.**

I. Introduction

THE two-stage opamp with Miller compensation [Fig. 1(a)] is widely utilized in analog systems, owing to its good noise performance, simple biasing, and large output-voltage swing [1]. However, in nanometer digital CMOS, the low supply voltages and the poor intrinsic gains of the MOS transistors complicate the low-power design of high-gain wide-swing opamps. Accordingly, this paper introduces a *gain-enhancement* technique (using *bulk biasing*) to increase the dc gain of the two-stage opamp, without affecting its output-voltage swing and without requiring any additional bias circuitry and, hence, power dissipation.

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For a process-insensitive design, the resistor in the Miller frequency-compensation network [the *RC* network in Fig. 1(a)] is typically implemented using an MOS transistor biased in triode. However, this approach cannot be implemented in low-voltage designs, at supply voltages[1] of $V_{\rm DD} \leq 3V_{\rm OV} + 2V_{\rm TH}$ (as described in Section III). Accordingly, this paper also introduces a *frequency-compensation* technique (based on a modified cascode-compensation approach), referred to as *pseudo cascode compensation*, to enable a process-insensitive design of the two-stage opamp at low supply voltages ($V_{\rm DD} = 1$ V in this experimental prototype), without requiring any additional power dissipation. Furthermore, our experimental results (Section IV) confirm that the proposed frequency-compensation technique improves the opamp settling behavior, compared to using Miller compensation with equal total compensation capacitance and the same power dissipation. Moreover, with the proposed frequency-compensation technique, the stability (phase margin) of the opamp is robust to the scaling of its bias current. Note that current-scalable opamps are widely utilized in reconfigurable analog-to-digital converters (ADCs) [2]–[4].

To validate the proposed gain-enhancement and frequency-compensation techniques, four replicas of a two-stage opamp were fabricated on the *same die* in a 1-V 65-nm digital CMOS process:

1) one opamp replica (**OPAMP1**) uses classical Miller compensation and does not use gain enhancement;
2) one opamp replica (**OPAMP1b**) uses classical Miller compensation and incorporates the proposed gain-enhancement technique;
3) one opamp replica (**OPAMP2**) incorporates the proposed frequency-compensation technique and does not use gain enhancement;
4) one opamp replica (**OPAMP2b**) incorporates both the proposed frequency-compensation and gain-enhancement techniques.

The corresponding transistors in the above four opamps had equal sizes. Furthermore, all four opamps had equal total compensation capacitance and the same total power dissipation. The performance of the four opamps was then measured and compared. Accordingly, our experimental results (Section IV) demonstrate that, compared to OPAMP1, OPAMP2b shows an enhancement of 12 dB in its dc gain and an improvement of 33% in its large-signal settling times, while maintaining the

[1]Here, to illustrate the performance trends, the opamp transistors are modeled using the square-law MOSFET model, with $V_{\rm TH}$ being the MOSFET threshold voltage and $V_{\rm OV} \equiv V_{\rm GS} - V_{\rm TH}$ being its overdrive (effective) voltage.

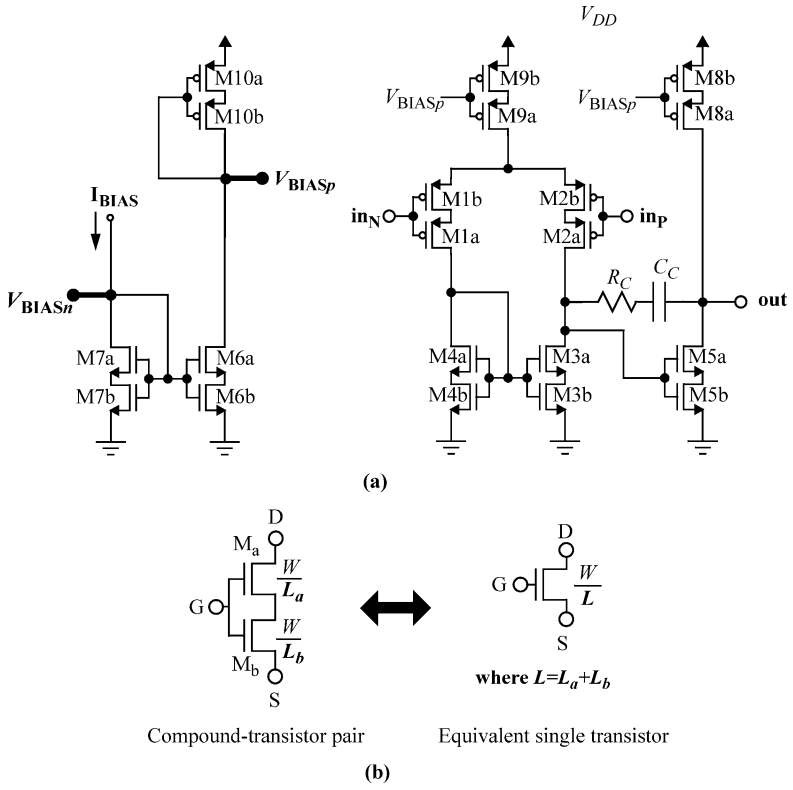


Fig. 1. (a) A Miller-compensated two-stage opamp with each of its transistors replaced by an equivalent compound-transistor pair, as per the transistor equivalency shown in Fig. 1(b). Here, the bulk terminal of each MOSFET is connected to its source terminal. Note that only $V_{\mathrm{BIAS}p}$ is required for biasing this single-ended-output opamp configuration. However, since opamps are typically configured with differential outputs, both $V_{\mathrm{BIAS}p}$ and $V_{\mathrm{BIAS}n}$ are typically required for biasing the opamp.

same output-voltage swing. Furthermore, the bias current of OPAMP2b can be scaled by a factor of 100, without affecting its phase margin.

Section II describes the proposed technique for dc-gain enhancement (using bulk biasing) and Section III presents the proposed technique for pseudo cascode compensation of the two-stage opamp. Section IV summarizes the experimental results.

II. Gain-Enhancement Technique Using Bulk Biasing

This section introduces an enhancement technique (using bulk biasing) for the dc gain of a two-stage opamp. For simplicity, this technique is described for a two-stage opamp with a single-ended output, although it is equally applicable to two-stage opamps with differential outputs.

A. Bulk Biasing

Consider the two-stage opamp with Miller compensation in Fig. 1(a). Note that each pair of compound transistors M_{Ka}–M_{Kb} $(K = 1, \ldots, 10)$ has an *I–V* characteristics equivalent to that of a single transistor M_K (with channel length $L_K = L_{Ka} + L_{Kb}$), as depicted in Fig. 1(b) [5], [6]. For simplicity, assume that overdrive voltages $V_{\mathrm{OV},K}$ of equivalent transistors M_K $(K = 1, \ldots, 10)$ have the same value, denoted as V_{OV}. Then, the opamp in Fig. 1(a) requires a supply voltage of $V_{\mathrm{DD}} \geq V_{\mathrm{GS5}} + V_{\mathrm{OV},2} + V_{\mathrm{OV},9} = V_{\mathrm{TH}} + 3V_{\mathrm{OV}}$.

In an nMOS compound-transistor pair [composed of M_a and M_b, as in Fig. 1(b)] whose equivalent single transistor is operating in saturation, transistor M_a operates in saturation while transistor M_b operates in triode. The threshold voltage $V_{\mathrm{TH}a}$ of M_a can be decreased by applying a voltage V_{Ba} to its bulk,[2] such that its bulk-source voltage $V_{\mathrm{BS}a}$ becomes greater than zero. Since M_a is operating in saturation, its overdrive voltage $V_{\mathrm{OV}a} = V_{\mathrm{GS}a} - V_{\mathrm{TH}a}$ is almost entirely fixed by its drain current and, hence, decreasing $V_{\mathrm{TH}a}$ through bulk biasing decreases its gate-source voltage $V_{\mathrm{GS}a}$. Since M_b is operating in triode, such decrease in $V_{\mathrm{GS}a}$ slightly increases[3] the drain-source voltage $V_{\mathrm{DS}b}$ of M_b. Furthermore, since M_b is not typically in deep triode, such slight increase in $V_{\mathrm{DS}b}$ moves M_b from triode to the edge of saturation, thereby noticeably increasing its output impedance. This results in the following two advantages for a compound-transistor pair with the proposed bulk biasing:

1) ***Output impedance:*** Owing to the increase in the output impedance of M_b, the overall output impedance $R_{\mathrm{out\_BB}}$ of the compound-transistor pair with the proposed bulk biasing is noticeably larger than the output impedance R_{out} of its equivalent single transistor without bulk biasing.

2) ***Short-circuit transconductance:*** Let g_{m_BB} denote the short-circuit transconductance of the compound-transistor pair with the proposed bulk biasing, while g_m denotes the short-circuit transconductance of its equivalent single transistor without bulk biasing. Since the output impedance of M_b is effectively the source resistance of M_a, increasing it

[2]Note that such bulk biasing is feasible for nMOS transistors, owing to the availability of a deep N-well in most nanometer CMOS processes.

[3]This can be easily shown using the square-law MOSFET model equations for M_a and M_b.

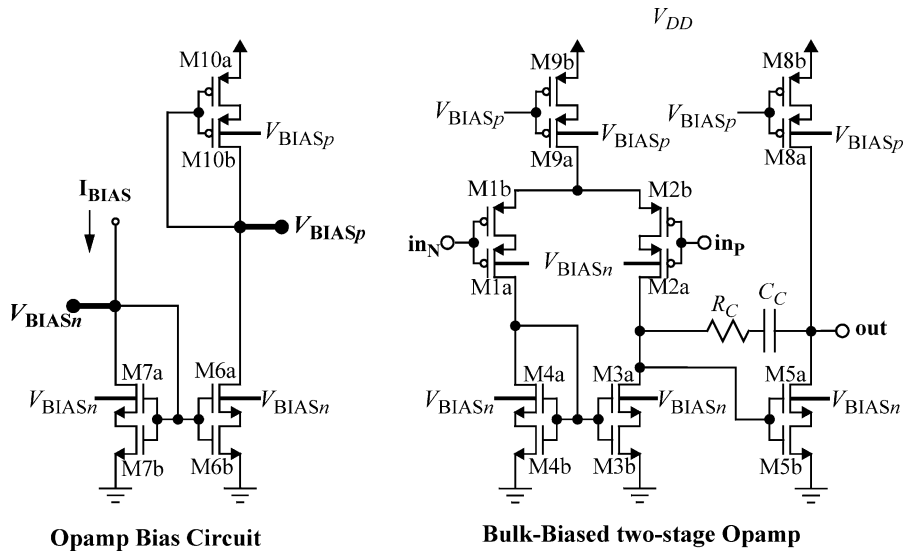


Fig. 2. Proposed bulk-biasing technique for the gain enhancement of the two-stage opamp in Fig. 1(a). Unless shown otherwise, the bulk terminal of each MOS transistor is connected to its source terminal.

degenerates the transconductance gain of M_a. Therefore, g_{m_BB} will be dominated by the short-circuit transconductance g_{mb} of M_b which is now operating at the edge of saturation. Since the channel length of the equivalent single transistor is larger than that of M_b (i.e., $L > L_b$), its short-circuit transconductance is smaller than that of M_b (i.e., $g_m < g_{mb}$). Hence, g_{m_BB} ($\cong g_{mb}$) is larger than g_m.

Similarly, the output impedance and short-circuit transconductance of a pMOS compound-transistor pair [composed of M_a and M_b, as in Fig. 1(b)] can be noticeably increased by applying a voltage V_{Ba} to the bulk of M_a, such that its source-bulk voltage V_{SBa} becomes grater than zero and, hence its threshold voltage $|V_{\mathrm{THa}}|$ is decreased.

The only constraint on voltage V_{Ba} used for bulk-biasing transistor M_a in a compound-transistor pair is that it should not turn on the bulk-source diode of M_a over all process, supply-voltage, and temperature corners. This constraint can be easily satisfied in low-voltage nanometer CMOS technologies, as described in the next subsection where the bulk-biasing technique proposed here for increasing the output impedance and short-circuit transconductance of a compound-transistor pair will be utilized to enhance the dc gain of the two-stage opamp in Fig. 1(a).

B. Proposed Two-Stage Opamp With Bulk Biasing

The proposed bulk-biasing technique described in the previous subsection is applied to all compound-transistor pairs of the two-stage opamp of Fig. 1(a), in order to increase the output impedance of its first and second gain stages and, hence, enhance its overall dc gain. Furthermore, for accurate biasing, the transistors in the opamp's bias circuit are bulk biased, using the same bias voltages as those used for bulk biasing the transistors in the opamp's gain stages. Fig. 2 shows the resulting opamp and its bias circuit. Observe that no additional bias circuitry is required for bulk biasing the two-stage opamp in Fig. 2, as $V_{\mathrm{BIAS}n}$ and $V_{\mathrm{BIAS}p}$ [which are available in the bias circuit of the classical two-stage opamp[4] in Fig. 1(a)] are used for bulk biasing.

Besides not requiring any additional bias circuitry, using $V_{\mathrm{BIAS}n}$ and $V_{\mathrm{BIAS}p}$ for bulk biasing (as proposed in Fig. 2) ensures that the source-bulk diodes of all opamp's transistors do not turn on over all process, supply-voltage, and temperature corners. To view this, assume, for simplicity, that all opamp's transistors M_{Kb} (for $K = 1, \ldots, 10$) in Fig. 2 have the same overdrive voltage, denoted as $V_{\mathrm{OV}b}$. As explained in the previous subsection, the proposed bulk-biasing technique moves transistors M_{Kb} (for $K = 3, \ldots, 7$) from triode to the edge of saturation. Hence, their drain-source voltages can be approximated as $V_{\mathrm{DS}b} = V_{\mathrm{OV}b}$. Thus, these transistors all have a drain-terminal voltage of $V_D \cong V_{\mathrm{OV}b}$, resulting in nMOS transistors M_{Ka} (for $K = 3, \ldots, 7$) all having a source-terminal voltage of $V_S \cong V_{\mathrm{OV}b}$. Therefore, since $V_{\mathrm{BIAS}n} \cong V_{\mathrm{OV}b} + V_{\mathrm{TH}n0}$, connecting the bulk terminal of nMOS transistors M_{Ka} (for $K = 3, \ldots, 7$) to $V_{\mathrm{BIAS}n}$ increases their bulk-source voltages to $V_{\mathrm{BS}} = V_{\mathrm{BIAS}n} - V_{\mathrm{OV}b} \cong V_{\mathrm{TH}n0}$ (where $V_{\mathrm{TH}n0}$ is the zero-bias nMOS threshold voltage). Similarly, since $V_{\mathrm{BIAS}p} \cong V_{\mathrm{DD}} - (V_{\mathrm{OV}b} + |V_{\mathrm{TH}p0}|)$, connecting the bulk terminal of pMOS transistors M_{Ka} (for $K = 8, \ldots, 10$) to $V_{\mathrm{BIAS}p}$ increases their source-bulk voltages to $V_{\mathrm{SB}} \cong |V_{\mathrm{TH}p0}|$ (where $|V_{\mathrm{TH}p0}|$ is the zero-bias pMOS threshold voltage). The values of $V_{\mathrm{TH}n0}$ and $|V_{\mathrm{TH}p0}|$ are independent of V_{DD}. Furthermore, in general-purpose nanometer CMOS transistors, their values are always (over all process corners) less than the voltage needed to turn-on the bulk-source diodes of the MOSFETs. Accordingly, the bulk-biasing technique proposed in Fig. 2 for transistors M_{Ka} (for $K = 3, \ldots, 10$) ensures that the source-bulk diodes of these transistors M_{Ka} remain always off. As for pMOS input transistor M_{1a} (whose drain-terminal voltage is $V_{\mathrm{OV}b} + V_{\mathrm{TH}n0} \cong V_{\mathrm{BIAS}n}$), connecting its bulk

[4]As noted in Fig. 1, only $V_{\mathrm{BIAS}p}$ or $V_{\mathrm{BIAS}n}$ is required for biasing a two-stage opamp with single-ended output. However, since opamps are typically configured with differential outputs, both $V_{\mathrm{BIAS}p}$ and $V_{\mathrm{BIAS}n}$ are effectively required for biasing.

terminal to $V_{\mathrm{BIAS}n}$ results in its source-bulk voltage being equal to its source-drain voltage (i.e., $V_{\mathrm{SB}1a} = V_{\mathrm{SD}1a}$). Due to the low V_{DD} in nanometer CMOS, the $|V_{\mathrm{SD}}|$ voltages of the transistors in the opamp's input stage must be relatively small, in order to ensure that these transistors operate in the active mode, over all process corners. Accordingly, $V_{\mathrm{SD}1a}$ is low enough and, hence, setting $V_{\mathrm{SB}1a} = V_{\mathrm{SD}1a}$ ensures that the source-bulk diode of M_{1a} will remain always off. The same argument can be extended to input transistor M_{2a}.

In summary, the proposed bulk-biasing technique for the two-stage opamp in Fig. 2 does not require any additional bias circuitry and, hence, power dissipation. Furthermore, our experimental results in Section IV demonstrate that this bulk-biasing technique increases the opamp's dc gain (by a factor of 4) and its unity-gain frequency ω_t (by 22%), while negligibly (less than 1%) affecting its output-voltage swing. This increase in ω_t can be explained as follows. The unity-gain frequency of a two-stage opamp with a dominant pole due to C_C [as in Fig. 1(a)] is

$$\omega_t = \frac{g_{m1}}{C_C} \tag{1}$$

where g_{m1} is the short-circuit transconductance of the single-transistor equivalent of compound-transistor pair M_{1a}–M_{1b}. Since the proposed bulk-biasing technique in Fig. 2 increases the opamp's g_{m1} (as explained in the previous subsection), it also increases its ω_t. Note that a drop in the opamp's phase margin is expected when its ω_t is increased. However, in the next section, a frequency-compensation technique is introduced for the two-stage opamp with the proposed bulk biasing. Compared to Miller compensation, the advantages of this frequency-compensation technique include improving the opamp's phase margin, while further improving its ω_t (as demonstrated by the experimental results in Section IV).

The input-referred thermal noise of the opamp in Fig. 1(a) (due to the thermal noise of its first stage, as the noise contribution of its second stage is relatively negligible) can be expressed as [7]

$$P_{n,\mathrm{in}} = \frac{16kT}{3}\frac{1}{g_{m1}}\left(1+\frac{g_{m4}}{g_{m1}}\right) \tag{2}$$

where k is the Boltzmann's constant, T is the absolute temperature in Kelvins, and g_{mK} is the short-circuit transconductance of the single-transistor equivalent of compound-transistor pair M_{Ka}–M_{Kb} (for $K = 1, 4$). Although g_{mK} is increased by applying the proposed bulk-biasing technique in Fig. 2 (as explained in the previous subsection), the ratio g_{m4}/g_{m1} remains approximately constant and, hence, $P_{n,\mathrm{in}}$ is not increased by applying the proposed bulk-biasing technique.

The common-mode rejection ratio (CMRR) of the two-stage opamp in Fig. 1(a) and the power-supply rejection ratio (PSRR) of its first stage[5] are proportional to the output impedance $R_{\mathrm{out}9}$ of compound-transistor pair M_{9a}–M_{9b}, which forms the tail current source for the input differential pair. Since the proposed bulk-biasing technique increases the output impedance of a compound-transistor pair (as explained in the previous subsection), applying this bulk-biasing technique to M_{9a}–M_{9b} (as in Fig. 2) increases $R_{\mathrm{out}9}$ and, hence, the opamp's CMRR and PSRR.

[5]When input referred, the power-supply noise in the opamp's second stage is relatively insignificant, as it is attenuated by the gain of the first stage.

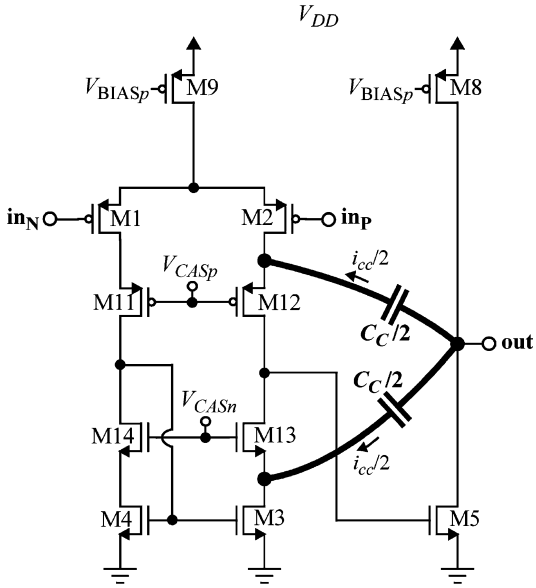


Fig. 3. *Classical* cascode compensation of a two-stage opamp. Note that $V_{\mathrm{CAS}p}$ and $V_{\mathrm{CAS}n}$ are the bias voltages for cascode transistors $M11$ to $M14$, and are generated in the opamp's bias circuit (Bias circuit not shown here).

III. Pseudo-Cascode Frequency Compensation

For the opamp's stability (phase margin) to be robust versus process and temperature variations, the opamp must be designed such that its dominant pole and zero frequencies are proportional to the short-circuit transconductance g_m of its MOS transistors. In a Miller-compensated two-stage opamp [Fig. 1(a)], this requires implementing the resistor in the Miller-compensation network using an MOS transistor, operated in triode with its gate voltage V_{GZ} adaptively changing with process and temperature variations. However, this approach is not suitable at low supply voltages, as it requires a $V_{\mathrm{GZ}} = 2(V_{\mathrm{OV}} + V_{\mathrm{TH}})$ and, hence, a $V_{\mathrm{DD}} \geq (3V_{\mathrm{OV}} + 2V_{\mathrm{TH}})$ to generate this V_{GZ} [7], [8]. Here, for simplicity, the equivalent transistors M_K of compound-transistor pairs M_{Ka}–$M_{Kb}(K = 1, \ldots, 10)$ in Fig. 1(a) are assumed to have the same overdrive voltage V_{OV} and threshold voltage V_{TH}. Accordingly, Miller compensation is not suitable for the low-voltage design of two-stage opamps that are insensitive to process and temperature variations.

At low V_{DD}, cascode compensation can be used to design an opamp whose pole/zero frequencies are proportional to the short-circuit transconductance g_m of its transistors [9]–[12]. Specifically, by designing the cascode-compensated opamp such that the g_m of all its transistors are derived from the same bias current I_{BIAS}, the opamp's pole/zero frequencies will be proportional to I_{BIAS}. Consequently, when I_{BIAS} changes due to process and temperature variations or is scaled for reconfigurability, the ratios of all opamp's pole and zero frequencies are not affected and, hence, the opamp's phase margin is preserved. Furthermore, cascode compensation achieves a higher power-supply-rejection ratio (PSRR) [9], [10] and a higher second-pole frequency (hence, a higher phase margin) [11] for the opamp, compared to Miller compensation.

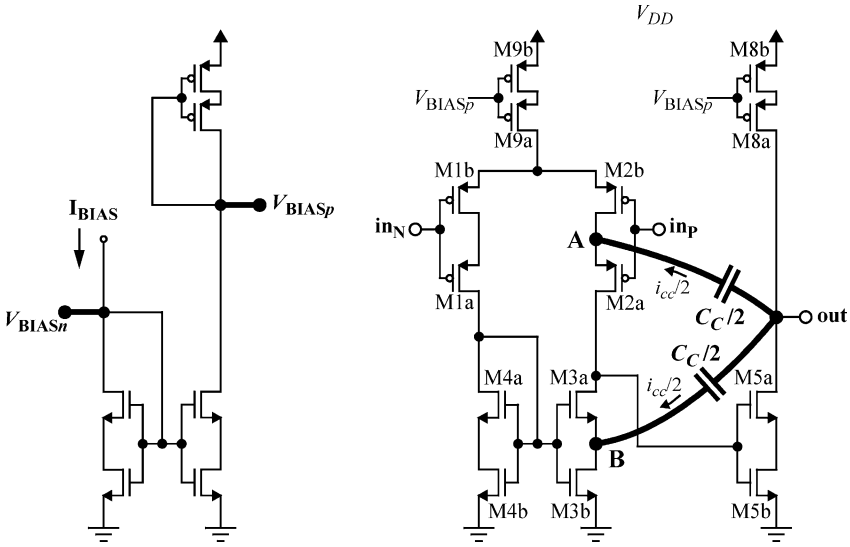


Fig. 4. Proposed *pseudo*-cascode compensation of the two-stage opamp in Fig. 1(a).

In cascode compensation, a compensation capacitor C_C is placed between the two-stage opamp output $V_{\rm out}$ and a virtual GND, with the current flowing through C_C (i.e., $i_{cc} = C_C(\mathrm{d}v_{\rm out})/(\mathrm{d}t)$) feeding back to the output of the opamp's first gain stage [9]–[12]. Fig. 3 shows a two-stage opamp with *classical* cascode compensation [11]. Here, compensation capacitor C_C is split, with one half connected to the cascode node of the cascoded input transistors and the other half connected to the cascode node of the cascoded active load. As described next, a *pseudo*-cascode compensation technique is introduced in this work to achieve the advantages of *classical*-cascode compensation methods, while enabling a low-voltage and a low-power design of the two-stage opamp. For simplicity, this technique will be described for a two-stage opamp with a single-ended output, although it is equally applicable to two-stage opamps with differential outputs.

A. Pseudo Cascode Compensation in a Two-Stage Opamp

Consider the two-stage opamp in Fig. 1(a). Recall (from Section II) that transistors M_{2a} and M_{3a} are operating in saturation. Therefore, by designing these transistors to have large short-circuit transconductances, their source terminals become low-impedance nodes and, hence, can be assumed to be at virtual GND. Accordingly, as proposed in Fig. 4, two compensation capacitors (each half the required C_C) can be connected between the opamp output $V_{\rm out}$ and these nodes (labeled A and B in Fig. 4).[6] Thus, the current flowing through these compensation capacitors (i.e., $i_{cc} = C_C(\mathrm{d}v_{\rm out})/(\mathrm{d}t)$) feeds back from the opamp's output to the output of its first gain stage through the sources of transistors M_{2a} and M_{3a}, as with cascode compensation. However, a small portion of i_{cc} will be lost through the drains of transistors M_{2b} and M_{3b}, thereby not reaching the output of the opamp's first gain stage. Though insignificant, this lost portion of i_{cc} is larger than the portion of i_{cc} lost through the drains of transistors M_2 and M_3 in a two-stage opamp with *classical* cascode compensation (Fig. 3). This is because M_2 and M_3 are biased in saturation when using classical cascode compensation (Fig. 3), while M_{2b} and M_{3b} are operating in triode when using the proposed compensation technique (Fig. 4). This is why the proposed compensation technique in Fig. 4 will be referred to as *pseudo* cascode compensation.

The main advantages of the proposed *pseudo*-cascode compensation (Fig. 4) over *classical* cascode compensation (Fig. 3) are as follows:

1) *Lower* $V_{\rm DD}$: For simplicity, assume that, in the two-stage opamp, all transistors operating in saturation have the same overdrive voltage, denoted $V_{\rm OV}$. In a two-stage opamp with classical cascode compensation (Fig. 3), cascode transistors M_{11} to M_{14} are biased in saturation. This requires a $V_{\rm DD} \geq V_{\rm GS5} + V_{\rm OV,12} + V_{\rm OV,2} + V_{\rm OV,9} = V_{\rm TH} + 4V_{\rm OV}$. In contrast, since the two-stage opamp with the proposed pseudo-cascode compensation (Fig. 4) has the same dc behavior as the two-stage opamp in Fig. 1(a), it only requires a $V_{\rm DD} \geq V_{\rm TH} + 3V_{\rm OV}$ (as derived in Section II). Accordingly, the minimum $V_{\rm DD}$ required when using the proposed pseudo-cascode compensation technique is lower by $V_{\rm OV}$, than that required when using classical-cascode compensation [9]–[12].

2) *Lower power*: In a two-stage opamp with classical cascode compensation (Fig. 3), a complex bias circuitry is required to generate the gate voltages of cascode transistors M_{12} and M_{13} (i.e., $V_{\rm CAS}p$ and $V_{\rm CAS}n$ in Fig. 3), such that transistors M_2 and M_3 are biased in saturation. However, in the two-stage opamp with the proposed pseudo-cascode compensation (Fig. 4), the gate terminals of transistors M_{2a} and M_{3a} are connected to those of M_{2b} and M_{3b} and, hence, no bias circuitry is required to generate the gate voltages of M_{2a} and M_{3a}. Accordingly, less power dissipation is required in this opamp.

[6]While the full compensation capacitance C_C can be connected between the opamp output and either node A or B, capacitance C_C is split in this experimental prototype (with one half connected to node A and the other half connected to node B), in order to demonstrate that both nodes A and B can be used for cascode compensation.

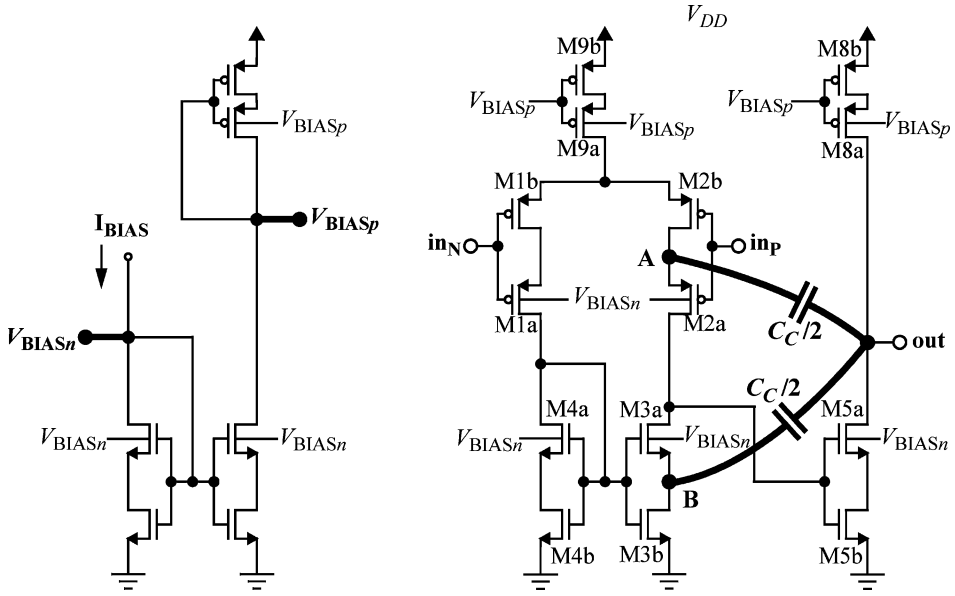


Fig. 5. Applying the proposed bulk-biasing technique to the two-stage opamp with pseudo cascode compensation in Fig. 4.

3) *Higher* ω_t: In Fig. 3, transistors M_2 and M_3 are biased in saturation. However, in Fig. 4, transistors M_{2b} and M_{3b} operate in triode and, hence, have a lower output resistance (as per Section II.A). This results in a slightly higher unity-gain frequency for the two-stage opamp with pseudo cascode compensation (Fig. 3) versus classical cascode compensation (Fig. 4), as can be readily proven by following the derivations presented in [11] for classical cascode compensation.

On the other hand, the two-stage opamp with the proposed pseudo-cascode compensation in Fig. 4 (where M_{2b} and M_{3b} are operating in triode) is expected to have a dc gain lower than that of the two-stage opamp with classical cascode compensation in Fig. 3 (where M_2 and M_3 are operating in saturation). This is the trade-off needed to enable designing a two-stage opamp with cascode compensation at low supply voltages and with lower power dissipation. Note that this dc gain can be enhanced by applying the proposed bulk-biasing technique (Section II) to the two-stage opamp with the proposed pseudo-cascode compensation, as described next.

B. Bulk Biasing of a Two-Stage Opamp With Pseudo Cascode Compensation

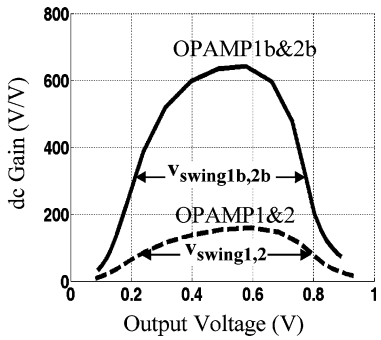
The proposed bulk-biasing technique (Section II) can be directly applied to the two-stage opamp with the proposed pseudo-cascode compensation, as shown in Fig. 5. This enables enhancing its dc gain by a factor of 4 (12 dB), as confirmed by our experimental results (Section IV). The trade off is a drop in its phase margin, due to a noticeable increase in its unity-gain frequency ω_t (by 30% in this experimental prototype) after applying the proposed bulk biasing. Yet, phase-margin drop due to bulk biasing in an opamp with pseudo cascode compensation (Fig. 5) is noticeably lower than that in a Miller-compensated opamp (Fig. 2), as confirmed by our experimental results. This is a direct result of cascode compensation providing a higher second-pole frequency than Miller compensation [11]. Furthermore, in an opamp with pseudo cascode compensation, applying the proposed bulk-biasing technique (Fig. 5) moves transistors M_{2b} and M_{3b} from triode to the edge of saturation and, hence, a more accurate cascode compensation (i.e., better pole splitting) is realized than without such bulk biasing (Fig. 4).

It is important to point out here that, when the proposed bulk-biasing technique is applied to the two-stage opamp with pseudo cascode compensation in Fig. 4 (as shown in Fig. 5), voltages $V_{\mathrm{DS5}b}, V_{\mathrm{SD2}b}$, and $V_{\mathrm{SD9}b}$ increase slightly, as transistors M_{5b}, M_{2b}, and M_{9b} are moved from triode to the edge of saturation. However, at a given opamp's bias current I_{BIAS}, increasing $V_{\mathrm{DS5}b}$ decreases $V_{\mathrm{GS5}b}$. Therefore, if the opamp in Fig. 4 is designed such that the increase in its $V_{\mathrm{SD2}b}$ and $V_{\mathrm{SD9}b}$ with bulk biasing (Fig. 5) is absorbed by the corresponding decrease in its $V_{\mathrm{GS5}b}$, then the minimum required V_{DD} (i.e., $V_{\mathrm{DD}} = (V_{\mathrm{GS5}b} + V_{\mathrm{SD2}a} + V_{\mathrm{SD2}b} + V_{\mathrm{SD9}a} + V_{\mathrm{SD9}b})$) will remain the same after applying the proposed bulk biasing (Fig. 5), as before applying such bulk biasing (Fig. 4). Furthermore, as noted in Section II and confirmed by our experimental results, applying the proposed bulk-biasing technique negligibly affects the output-voltage swing of the two-stage opamp.

IV. Experimental Results

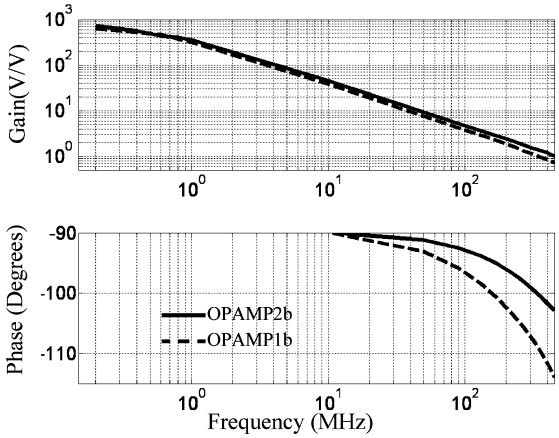
To demonstrate the performance enhancement achieved by applying the proposed bulk-biasing (gain-enhancement) technique and/or the proposed pseudo-cascode compensation technique to a two-stage opamp, four replicas of a two-stage opamp were fabricated on the *same die* in a 1-V 65-nm digital CMOS process:

1) One opamp replica (**OPAMP1**) uses classical Miller compensation and does not use gain enhancement, as in Fig. 1(a).
2) One opamp replica (**OPAMP1b**) uses classical Miller compensation and incorporates the proposed bulk-biasing technique, as in Fig. 2.



	OPAMP1	OPAMP1b	OPAMP2	OPAMP2b
Proposed Bulk-Biasing Technique	✘	✔	✘	✔
Compensation Technique	Miller	Miller	Pseudo Cascode	Pseudo Cascode

Fig. 6. Measured dc gain of each of the four fabricated opamps versus its output voltage.



	OPAMP1b	OPAMP2b
Proposed Bulk-Biasing Technique	✔	✔
Compensation Technique	Miller	Pseudo Cascode

Fig. 7. Measured open-loop frequency response (for $C_L = 2$ pF off-chip) of OPAMP1b (with Miller compensation) and OPAMP2b (with the proposed pseudo-cascode compensation).

3) One opamp replica (**OPAMP2**) incorporates the proposed frequency-compensation technique and does not use gain enhancement, as in Fig. 4.
4) One opamp replica (**OPAMP2b**) incorporates both our proposed frequency-compensation and bulk-biasing techniques, as in Fig. 5.

The corresponding transistors in all four opamps had equal sizes. Furthermore, all four opamps had equal total compensation capacitance C_C and the same total power dissipation. The bias circuits of the opamps had their transistors sized such that, when $V_{\mathrm{BIAS}n}$ and $V_{\mathrm{BIAS}p}$ are used for bulk biasing (in OPAMP1b and OPAMP2b), the source-bulk voltage $|V_{\mathrm{SB}}|$ of all transistors remains less than 450 mV over all process, supply-voltage, and temperature corners. This ensures that the source-bulk diode of all transistors does not turn on with any process, supply-voltage, and temperature variation. Miller-compensation resistors R_C in OPAMP1 and OPAMP1b were each optimized for best settling response and were fabricated using poly resistors. Compensation capacitors C_C were implemented using fringe capacitors.

Fig. 6 shows the measured dc gain of the four fabricated opamps versus their output voltage. Accordingly, applying the proposed bulk-biasing technique (in OPAMP1b and OPAMP2b versus OPAMP1 and OPAMP2) increases the opamp's dc gain by 12 dB or a factor of 4 (from 160 to 640 V/V), without affecting the output-voltage swing V_{swing}. Here, V_{swing} is defined as the difference between the maximum and minimum opamp's output voltages, at which the magnitude of the opamp's dc gain is $A_{0,\max}/2$ (where $A_{0,\max}$ is the maximum magnitude of the opamp's dc gain, over its full output-voltage swing). As per Fig. 6, the measured output-voltage swing is $V_{\mathrm{swing}} = 560$ mV after applying the proposed bulk-biasing technique (in OPAMP1b and OPAMP2b), while it was $V_{\mathrm{swing}} = 565$ mV before applying it (in OPAMP1 and OPAMP2).

Fig. 7 shows the measured open-loop frequency response[7] of OPAMP1b (using Miller compensation) and OPAMP2b (using the proposed pseudo-cascode compensation). The proposed bulk-biasing technique was applied to both opamps. Accordingly, in a two-stage opamp with the proposed bulk biasing, using the proposed pseudo-cascode compensation increases the opamp's unity-gain frequency (from 390 to 450 MHz) and its phase margin (from 71° to 77°).

Fig. 8 shows the large-signal-step ($V_{\mathrm{out\_step}} \approx V_{\mathrm{DD}}/2$) response of the four fabricated opamps. Accordingly, compared to Miller compensation (OPAMP1 and OPAMP1b), using the proposed pseudo-cascode compensation (OPAMP2 and OPAMP2b) improves the large-signal step response. Specifically, for a large positive output step, using the proposed pseudo-cascode compensation eliminates the opamp's large-signal overshoot and improves its large-signal rise settling time by up to 38%. For a large negative output step, using the proposed pseudo-cascode compensation improves the opamp's large-signal fall settling time by up to 27%. Observe that, for a positive output step (Fig. 8), the output of all opamps (in Figs. 1, 2, 4, and 5) is charged by the current source formed by transistors M_{8a}–M_{8b}, whose current is constant. However, for a negative output step, the output of all opamps is discharged by the current source formed by transistors M_{5a}–M_{5b}, whose current is not constant but rather controlled by the feedback path from the opamp's output (through C_F and the opamp's input stage) to the gate of current-source transistors M_{5a}–M_{5b}. This is why the large-signal step response of all opamps (Fig. 8) is slew-rate limited for a positive output step, but not for a negative output step. Hence, the large-signal fall settling time of all opamps is smaller than its rise counterpart.

Table I summarizes and compares the measured performance of the four fabricated opamps.

[7]To measure the opamp's open-loop frequency response, the opamp's input and output signals were acquired from the corresponding chip pins using 2.5-GHz active FET probes (Tektronix TAP2500) connected to a 2.5-GHz real-time digital oscilloscope (Tektronix DPO7254). By using high-bandwidth active probes and a real-time oscilloscope, the high-frequency gain- and phase-measurement errors are minimized. Furthermore, by placing the small contact tip of the active probes very close to the chip pins, any delay due to the PCB traces is minimized.

TABLE I
MEASURED PERFORMANCE OF THE FOUR FABRICATED OPAMPS

	OPAMP1	OPAMP1b	OPAMP2	OPAMP2b
Compensation Technique	Miller	Miller	Pseudo Cascode	Pseudo Cascode
Proposed Bulk-Biasing Technique	No	Yes	No	Yes
I_{BIAS} (mA)	0.4	0.4	0.4	0.4
Total power consumption @ V_{DD} = 1V (mW)	1.6	1.6	1.6	1.6
C_C (pF)	1	1	1	1
Unity-Gain Frequency (MHz)	320	390	345	450
Phase Margin (Degree)	84	71	84	77
Output-Voltage Swing V_{swing} (mV) *	565	560	565	560
DC Gain (V/V)	160	640	160	640
Overshoot in the Large-Signal Step Response (%)	6	12	0	0.5
1% Rise/Fall Settling Times (ns)	15 / 9	16 / 7	12 / 6.5	10 / 6

* Here, the opamp's output voltage swing $V_{\rm swing}$ is defined as the difference between the opamp's maximum and minimum output voltages, at which the magnitude of its dc gain is $A_{0,\max}/2$ (where $A_{0,\max}$ is the maximum magnitude of the opamp's dc gain, over its full output-voltage swing).

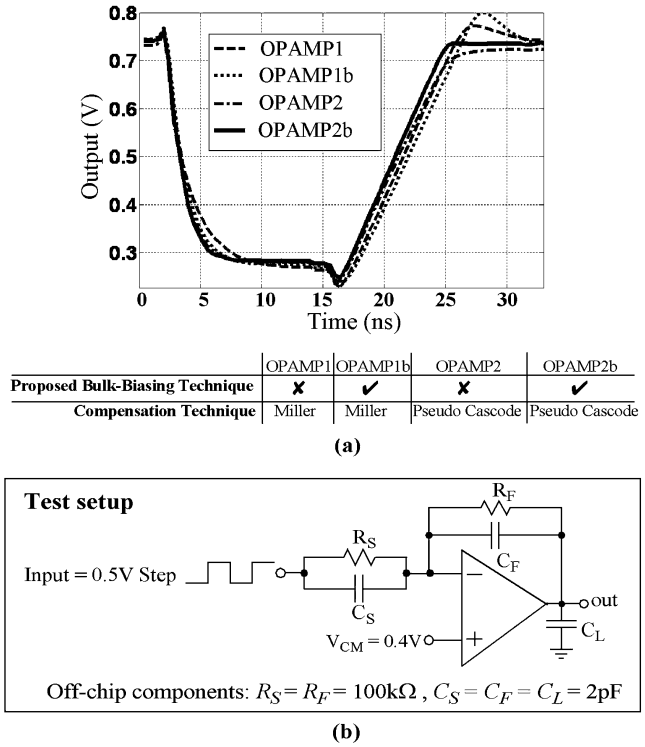


Fig. 8. (a) Measured large-signal step response of each of the four fabricated opamps, and (b) test setup used for this measurement.

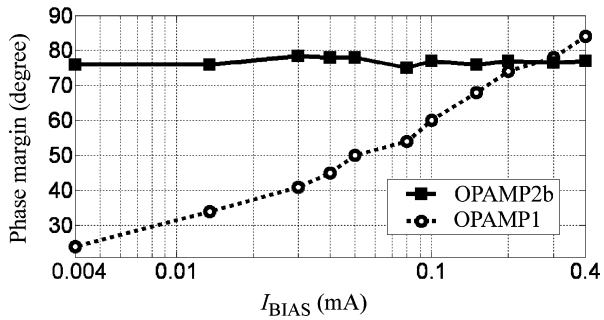


Fig. 9. Measured phase margin of OPAMP2b (with pseudo cascode compensation) and OPAMP1 (with Miller compensation) versus the opamp's bias current $I_{\rm BIAS}$. This demonstrates the robustness of the opamp's stability (versus the scaling of its $I_{\rm BIAS}$) achieved by using the proposed pseudo-cascode compensation technique.

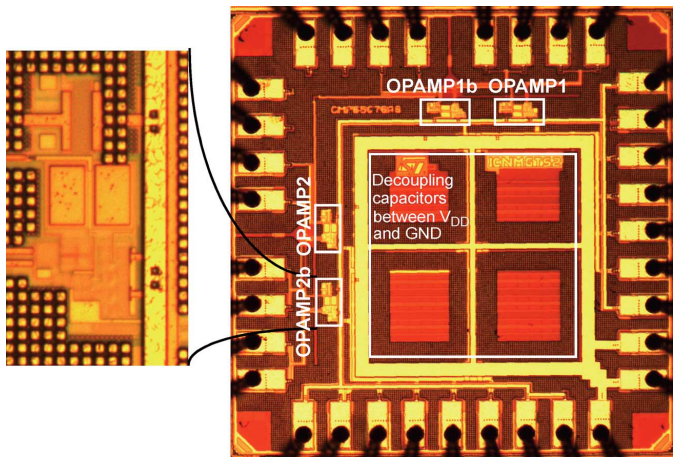


Fig. 10. Chip micrograph (along with a zoom-in on the area of OPAMP2b), fabricated in a 1-V 65-nm digital CMOS process.

Fig. 9 compares the measured phase margin of OPAMP1 (with Miller compensation) and OPAMP2b (with the proposed pseudo-cascode compensation) versus the opamp's bias current $I_{\rm BIAS}$. Accordingly, the proposed pseudo-cascode compensation technique enables maintaining a constant phase margin for the opamp, while its $I_{\rm BIAS}$ is scaled by a factor of 100 (from 4 to 400 μA).

Fig. 10 shows the micrograph of the chip where all four opamps were fabricated in a 1-V 65-nm digital CMOS process. All four opamps occupied the same active area of 1800 μm^2.

V. CONCLUSION

First, a pseudo-cascode compensation technique was proposed to design a process-insensitive and current-scalable two-stage opamp at low supply voltages. Compared to Miller

compensation with the same compensation capacitor, the proposed pseudo-cascode compensation improves the opamp's unity-gain frequency and its large-signal settling response, while enabling its low-voltage implementation without requiring any additional power dissipation. Compared to classical cascode compensation, this pseudo-cascode compensation reduces the required supply voltage and the required power dissipation. Second, a bulk-biasing technique was proposed to enhance the dc gain of a two-stage opamp, without affecting the achieved output-voltage swing nor the required supply voltage and power dissipation. The fabricated prototypes in a 1-V 65-nm digital CMOS process demonstrated that, compared to using Miller compensation, applying the proposed frequency-compensation and bulk-biasing techniques to a two-stage opamp increases its dc gain (by a factor of 4 or 12 dB) and its unit-gain frequency (by 40%). Furthermore, the opamp's phase margin can be maintained over a factor of 100 scaling in its bias current. Moreover, the overshoot in the opamp's large-signal step response is eliminated and the rise/fall settling times are improved by 33%. Importantly, this is all achieved with a minimal drop in the opamp's phase margin and without affecting the opamp's output-voltage swing nor requiring any additional power dissipation.

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