# A Reconfigurable 10-12b 0.4-44MS/s Pipelined ADC with 0.35-0.5pJ/step in 1.2V 90nm Digital CMOS

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*Abstract*- **This pipelined ADC is reconfigurable over sampling frequencies of 0.4-44 MS/s and resolutions of 10-12 bits, thus targeting multi-standard wireless terminals. Fabricated in 1.2-V 90-nm digital CMOS, it achieves a competitive FOM of 0.35-0.5 pJ/conversion step over its wide reconfigurability space. For power scalability, the ADC bandwidth and resolution are reconfigured using current-scaling and stage-bypass methods, respectively. The following techniques are also introduced to achieve this low-power performance for the ADC over its wide reconfigurability space, and to enable its implementation in low-voltage nanometer CMOS: 1) pseudo-cascode compensation for the low-power design of low-voltage current-scalable opamps; 2) design of switched-capacitor dynamic comparators with low input loading; 3) low-power digital background gain calibration to enable designing the ADC using low-gain/low-power opamps.**

## I. Introduction

The growing demand for multi-mode/multi-standard wireless terminals is fuelling interest in ADCs that are reconfigurable over a wide range of bandwidths $BW$ and resolutions $N$. Furthermore, for power-efficiency, these ADCs must be power-scalable (i.e., their power scales with their $BW$ and $N$), thereby maintaining a constant figure-of-merit (FOM) over their entire reconfigurability space.

A ΔΣ ADC can only be reconfigured to *discrete* bandwidth-resolution modes (covering specific radio standards), due to the strong interdependence between its bandwidth and its resolution. Thus, a pipelined ADC is more attractive for reconfigurability, as it can be reconfigured over a *continuous* range of bandwidths, for each setting of its resolution.

This pipelined ADC is reconfigurable over a continuous range of sampling frequencies $f_S$ = 0.4 to 44 MS/s (bandwidths $BW$ = 0.2 to 22 MHz), for resolutions $N$ = 10,11,12 bits. Fabricated in 1.2-V 90-nm digital CMOS, it achieves an $\text{FOM} \equiv \text{power}/(f_S \cdot 2^{\text{ENOB}})$ = 0.35 to 0.5 pJ/step over its full bandwidth-resolution space. Thus, this ADC is suitable for multiple wireless and cellular standards, ranging from GSM up to LTE/WiMax and 802.11g. Furthermore, owing to its power efficiency, this ADC is attractive for various applications over a wide bandwidth-resolution space, thereby saving on development costs and reducing the time-to-market.

Compared to the state-of-the-art power-efficient *reconfigurable* pipelined (Fig. 10a) or ΔΣ (Fig. 10b) ADCs, this ADC provides a wide bandwidth-resolution reconfigurability space, while maintaining the most competitive FOM over this entire space. Furthermore, at its maximum speed and maximum resolution setting, this ADC achieves an FOM that is among the most competitive compared to the FOMs of *non-reconfigurable* pipelined ADCs with 10.5 to 11.5 ENOBs (Fig. 11).

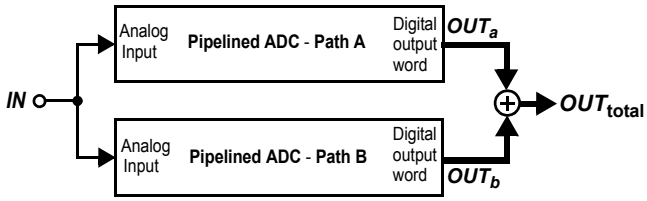



**Fig. 1** The 2-path ADC formed by 2 identically-designed pipelined ADCs.

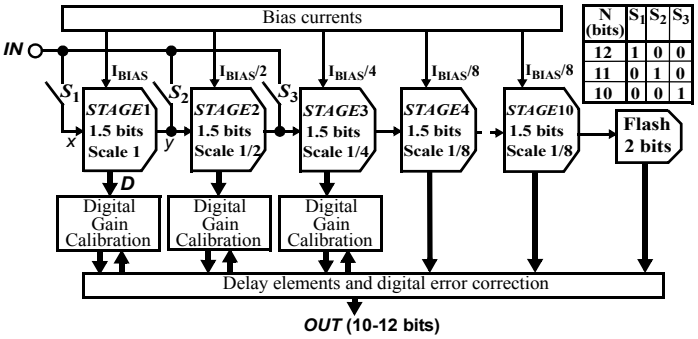



**Fig. 2** One path of this reconfigurable 2-path pipelined ADC. The table shows the state of switches $S_1$-$S_3$ for each ADC resolution $N$.

The **low-power** performance of this ADC over its wide reconfigurability space and its implementation in a **low-voltage** nanometer CMOS process were enabled through the introduction of the following techniques:

**1) Pseudo-cascode compensation** for the low-power design of low-voltage current-scalable opamps (Section III.A);

**2)** Design of switched-capacitor **dynamic comparators with low input-loading** (Section III.B);

**3) Low-power digital background calibration** to enable the ADC design using low-gain/low-power opamps (Section IV).

## II. ADC Architecture

This ADC is realized using 2 identically-designed pipelined ADCs, which are then interconnected to form a 2-path (split) ADC, as in Fig. 1. Splitting the ADC into two identical ADCs does not increase its total power or area [1], while it enables implementing our gain-calibration technique (Section IV).

Each ADC path consists of ten 1.5-bit pipeline stages and a 2-bit flash (Fig. 2). To minimize the ADC power, *STAGE*1-4 are each scaled down by a factor of 2 relative to the preceding stage. *STAGE*4-10 are identical. To achieve the targeted resolution, digital gain calibration is used in *STAGE*1-3.

The ADC resolution $N$ is reconfigured using stage-selection switches $S_k$ ($k$=1,2,3) to bypass the preceding stages (Fig. 2). Figure 3 depicts the multiplying digital-to-analog converter (MDAC) used in pipeline *STAGE*1-3 in Fig. 2, including the associated switch $S_k$.When a pipeline stage is bypassed, it is

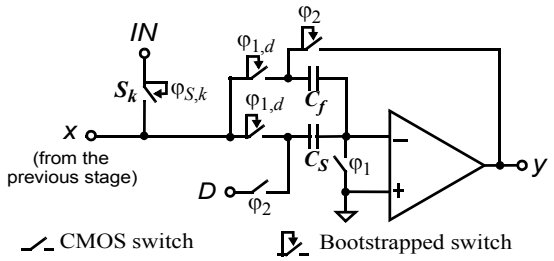



**Fig. 3** MDAC used in pipeline *STAGE*1-3 in Fig. 2, including the associated stage-selection switch $S_k$ (with $k$ = 1,2,3 corresponding to *STAGE*1,2,3, respectively). Two-phase non-overlapping clocks ($\varphi_1$, $\varphi_2$) and delayed clocks ($\varphi_{1d}$, $\varphi_{2d}$) are used with:

$$\varphi_{S,k} = \begin{cases} \varphi_{1d}, \text{ if switch } S_k \text{ in Fig. 2 is used to pass the input signal} \\ 0, \text{ otherwise} \end{cases}$$

Here, a single-ended implementation is shown for simplicity.

switched off (by turning off its opamp biasing circuit) to save power. Furthermore, the clock phase $\varphi_2$ going to its MDAC is set to zero, in order to disconnect the feedback capacitor $C_f$ from the MDAC residue output (Fig. 3). This turns the output of the bypassed pipeline stage into a floating node. Thus, when the ADC input signal is steered via switch $S_k$, the bypassed-stage output will not affect the next-stage input.

To achieve power scalability when $f_S$ is reconfigured, the bias current $I_{BIAS}$ to the opamp in each pipeline stage is linearly scaled with $1/f_S$.

## III. Circuit Implementation

### A. Opamps

Two-stage opamps are used here to maximize the swing at the residue output of the pipeline stages. When $f_S$ is reconfigured, the bias current $I_{BIAS}$ of the opamps is scaled to maintain a constant FOM. However, this can destabilize the opamps. To preserve the opamp stability (phase-margin) as its $I_{BIAS}$ is scaled, the opamp must be designed such that its dominant pole/zero frequencies scale proportionally with its $I_{BIAS}$. With Miller compensation, this requires implementing the resistor in series with the compensation capacitor using a triode transistor having its gate voltage $V_{GZ}$ adaptively changing with $I_{BIAS}$. However, this approach is not suitable at low $V_{DD}$, as it requires[1] a $V_{GZ} = 2(V_{eff} + V_t)$ and, hence, a $V_{DD} \geq 3V_{eff} + 2V_t$ to generate this $V_{GZ}$ [2].

At low $V_{DD}$, cascode compensation can be used to design an opamp whose pole/zero frequencies are proportional to its $I_{BIAS}$ [3]. This paper introduces a *pseudo* cascode compensation technique to improve the opamp's power efficiency and unity-gain bandwidth compared to when using classical cascode compensation. With *pseudo* cascode compensation (Fig. 4), compensation capacitor $C_C$ is placed between the opamp output and the sources of cascode transistors *M1a-M1b* (which are biased in saturation using $V_{G1}$), as with classical cascode compensation. However, with *pseudo* cascode compensation, $V_{G2}$ and $V_{G1}$ are connected to the same bias $V_{Bn}$, in order for *M1a-M1b* to force *M2a-M2b* into triode (rather than using a $V_{G2}$ different from $V_{G1}$ to bias

1. Here, $V_t$ is the threshold voltage of an MOS transistor and $V_{eff} \equiv V_{GS} - V_t$ is its effective (overdrive) voltage.

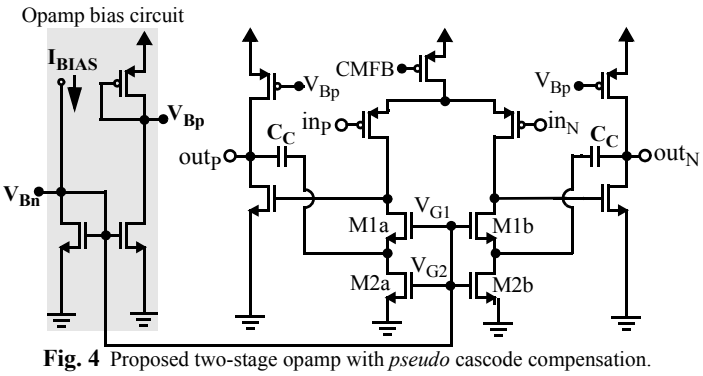



**Fig. 4** Proposed two-stage opamp with *pseudo* cascode compensation.

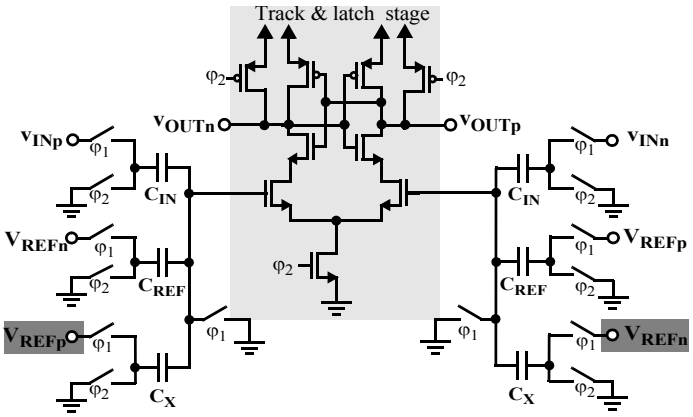



**Fig. 5** Dynamic comparator with branch $C_X$ added to lower $C_{IN}$.

*M2a-M2b* in saturation, as with classical cascode compensation). Thus, the advantages of *pseudo* cascode compensation are:

**1) Lower opamp power:** Given the large $f_S$ (hence $I_{BIAS}$) scaling range in this ADC, a large portion of the power of each opamp is dissipated in its bias circuit to provide good matching between the dc currents in the opamp branches and reference current $I_{BIAS}$. Therefore, noticeable savings in opamp power dissipation are achieved by eliminating one branch of its bias circuit, through connecting $V_{G1}$ and $V_{G2}$ to the *same* bias (Fig. 4).

**2) Higher opamp unity-gain bandwidth $\omega_t$:** When *M2a-M2b* are in triode with *pseudo* cascode compensation (rather than in saturation, as with classical cascode compensation), small-signal analysis shows that the opamp's phase margin is unchanged, while its $\omega_t$ is increased. Furthermore, noise analysis shows that the opamp's noise floor is decreased. Thus, with *pseudo* cascode compensation, the opamp's inband noise power remains almost constant, while its $\omega_t$ improves.

A drawback of pseudo cascode compensation is a drop in opamp dc gain, because *M2a-M2b* are operating in triode (rather than in saturation, as with classical cascode compensation). However, this is not a concern in this ADC, as gain errors due to the low dc gains of the opamps are digitally calibrated for in the background.

### B. Comparators

Figure 5 shows the dynamic comparator used in the sub-ADCs of the pipeline stages. Here, compared to a classical switched-capacitor dynamic comparator [4], branch $C_X$ is added to set the comparator's trip point at:

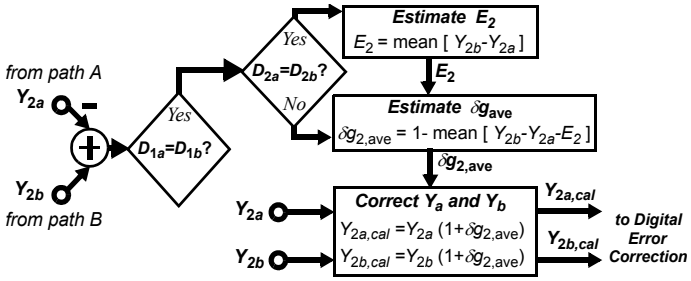



**Fig. 6** Block diagram of the digital calibration unit for pipeline *STAGE*2. Here, $D_2$ is the digital output of pipeline *STAGE*2, while $Y_2$ denotes its residue output signal as digitized by the subsequent pipeline stages. Subscripts *a* and *b* refer to paths A and B, respectively. Mean[.] denotes the averaging operation.

$V_C = [(C_{\mathrm{REF}} - C_X)/C_{\mathrm{IN}}]V_{\mathrm{REF}}$. Thus, for a minimum $C_{\mathrm{REF}}$ (e.g., set by parasitics), adding branch $C_X$ lowers the size of $C_{\mathrm{IN}}$ required to set a targeted $V_C$. This helps saving power, as the $C_{\mathrm{IN}}$ of the comparators in a pipeline stage loads the residue output of the previous pipeline stage.

## IV. Digital Background Gain Calibration

Digital background calibration of *gain* errors $\delta g$ (due to the finite gain of the opamps) is performed to enable designing the MDACs using low-gain/low-power opamps in standard 90-nm CMOS. *Capacitor-mismatch* errors are not calibrated, as the capacitor matching was sufficient for this 12-bit ADC.

In this 2-path ADC (consisting of paths A and B), the gain errors of *only* pipeline *STAGE*1-3 in both paths are calibrated, as the overall ADC performance is most sensitive to the nonidealities in its front-end stages. To concurrently calibrate *multiple* pipeline stages, we extended our low-power digital background calibration technique in [5], as described below.

The calibration technique in [5] requires the input to the stage under calibration in both ADC paths to be equal. Therefore, it is only directly applicable to *STAGE*1, as the input to any stage following *STAGE*1 may differ between the ADC paths (due to decision-point difference in the sub-ADCs of the previous pipeline stages between paths A and B). However, observe that, since the input to *STAGE*1 in both paths are equal, the residue output of *STAGE*1 (which forms the input of *STAGE*2) in paths A and B are equal when digital output *D* of *STAGE*1 in both paths are equal (i.e., $D_{1a}$=$D_{1b}$). Accordingly, the technique in [5] can be extended to calibrate for the gain error of *STAGE*2 (i.e., $\delta g_2$), if the calibration unit of *STAGE*2 estimates $\delta g_2$ *only* when $D_{1a}$=$D_{1b}$. The resulting digital calibration unit for pipeline *STAGE*2 is depicted in Fig. 6. The same concept can be extended to calibrate *STAGE*3. Accordingly, we utilized the calibration technique in [5] to concurrently calibrate *STAGE*1-3, with the calibration unit of *STAGE*2 estimating $\delta g_2$ only when $D_{1a}$=$D_{1b}$, and with the calibration unit of *STAGE*3 estimating $\delta g_3$ only when $D_{1a}$=$D_{1b}$ and $D_{2a}$=$D_{2b}$.

This digital background gain-calibration technique achieves **low power**, since: **1)** it does not require a pseudo-random (PN) signal generator, as it uses calibration signals with constant values, rather than PN values; and **2)** most of the functions inside the calibration units of *STAGE*1-3 can be shared between paths A and B of the 2-path ADC.

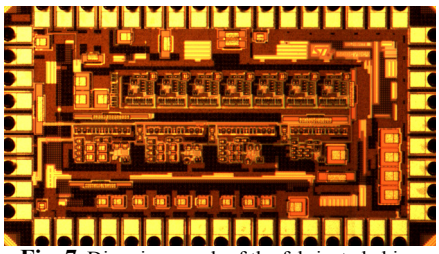


**Fig. 7** Die micrograph of the fabricated chip.

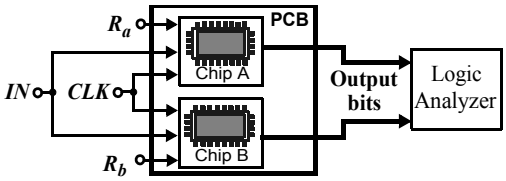



**Fig. 8** Experimental test setup.

## V. Test Setup

One path of this reconfigurable 2-path pipelined ADC is fabricated in *standard* 90-nm 1.2-V digital CMOS (Fig. 7). To realize the 2-path ADC, two ADC chips are mounted on the same PCB (Fig. 8). Both chips are then driven by the same input and clock signals, while different calibration signals $R_a$ and $R_b$ are used. The same power-supply voltages, bias currents, and reference voltages are applied to both chips. The digital outputs from each ADC path are then added to form the total output of the 2-path ADC. By fabricating only one path of the ADC and utilizing this test setup (Fig. 8), significant savings in prototyping (proof-of-concept) costs were achieved, compared to fabricating both ADC paths on the same die.

## VI. Experimental Results

Table I summarizes the measured performance of this two-path ADC at its minimum ($f_S$ = 0.4MS/s) and maximum ($f_S$ = 44MS/s) sampling frequencies for the various settings of its resolution ($N$ = 10,11,12 bits), when a full-scale sinusoid at the Nyquist frequency ( $f_{in} \cong f_S/2$ ) is applied at its input.

### *A. Power for Digital Calibration*

To estimate the power required for gain calibration, the digital calibration units were synthesized on a 1.2-V 90-nm FPGA. Observe that the power dissipation of the digital calibration unit can be substantially reduced through a custom silicon design, rather than an FPGA implementation. This can significantly improve the FOM of the ADC, as the power dissipation in the digital calibration units accounts for up to 41% of the total ADC power (Table I).

**TABLE I.** Measured performance (Process: 1.2-V 90-nm digital CMOS)

| **Resolution *N* (bits)** | | **10** | | **11** | | **12** | |
|---|---|---|---|---|---|---|---|
| **Sampling Frequency $f_S$ (MS/s)** | | **0.4** | **44** | **0.4** | **44** | **0.4** | **44** |
| Max. DNL (LSB) | | 0.5 | 0.8 | 0.6 | 0.8 | 0.8 | 0.9 |
| Max. INL (LSB) | | 0.4 | 1 | 0.6 | 1 | 0.8 | 1.26 |
| SNDR (dB) @ $f_{in} \approx f_S/2$ | | 60.9 | 59.1 | 63.4 | 62.1 | 66.6 | 65.1 |
| SFDR (dB) @ $f_{in} \approx f_S/2$ | | 82 | 66 | 78 | 73 | 78 | 79 |
| Analog Power(mW)@$V_{DD}$=1.2V | | 0.12 | 7.1 | 0.15 | 8.9 | 0.21 | 11.7 |
| Digital Power(mW) @ $V_{DD}$ = 1.2 V | Calibration | 0.028 | 3.1 | 0.056 | 6.2 | 0.085 | 9.3 |
| | Chip | 0.036 | 1.85 | 0.038 | 1.86 | 0.039 | 1.87 |
| Total Power (mW) @ $V_{DD}$=1.2V | | 0.184 | 12.05 | 0.244 | 16.96 | 0.334 | 22.87 |
| **FOM** (pJ/conv-step) | | **0.5** | **0.37** | **0.5** | **0.37** | **0.47** | **0.35** |

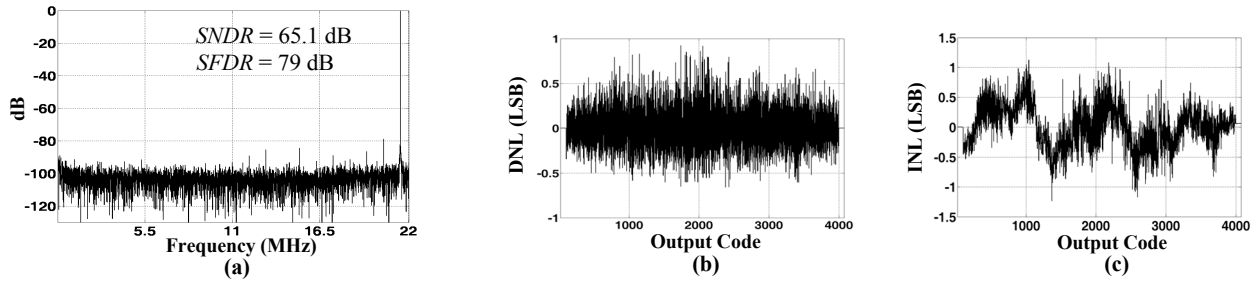



**Fig. 9** Measured: **(a)** output spectrum for $f_{in} \cong f_S/2$ ; **(b)** DNL; and **(c)** INL of this reconfigurable 2-path ADC at its maximum resolution and maximum sampling frequency ($N$ = 12 bits and $f_S$ = 44MS/s).

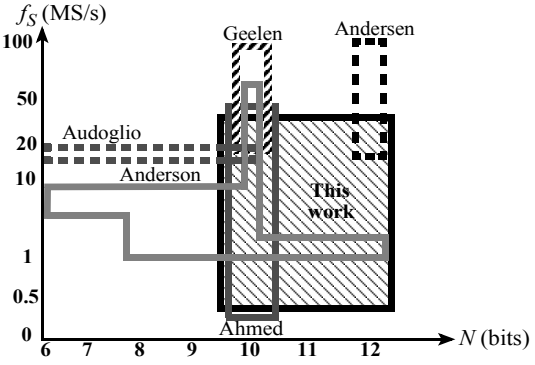
### *B. Measurement Plots*

Figure 9(a) shows the measured output spectrum for $f_{in} \cong f_S/2$ , when the ADC is configured to its maximum speed and resolution ( $f_S$ = 44 MS/s and $N$ = 12 bits ).

Figures 9(b) and 9(c) show the measured DNL/INL profiles for a full-scale sinusoidal input signal, when the ADC is configured to its maximum speed and maximum resolution ( $f_S$ = 44 MS/s and $N$ = 12 bits ). The maximum INL is 1.26 LSB and the maximum DNL is 0.9 LSB.

### *C. Performance Comparison*

Fig. 10 compares the performance of this ADC to the state-of-the-art power-efficient *reconfigurable* pipelined (Fig. 10a) and ΔΣ (Fig. 10b) ADCs. Accordingly, this ADC achieves a wide bandwidth-resolution reconfigurability space, while maintaining the most competitive FOM over this entire space. Furthermore, at its maximum speed and resolution setting, this ADC achieves an FOM that is among the most competitive compared to the FOM of *non-reconfigurable* pipelined ADCs with 10.5 to 11.5 ENOBs, as shown in Fig. 11.




| | Geelen ISSCC 06 | Audoglio ESSCIRC 06 | Ahmed JSSC July 08 | Andersen JSSC July 05 | Anderson VLSI 05 | **This work** |
|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.2V | 1.8V | 1.8V | 1.8V | 1.8V | **1.2V** |
| CMOS | 90nm | 0.13μm | 0.18μm | 0.18μm | 0.18μm | **90nm** |
| FOM (pJ/conversion step) | 0.5-0.7 | 0.9-5.1 | 1.5-6 | 0.66-0.82 | 2-107 | **0.35-0.5** |

**(a) Comparison to reconfigurable pipelined ADCs**

| | Bandwidth modes (MHz) | CMOS process (nm) | Supply Voltage (V) | FOM (pJ/step) |
|---|---|---|---|---|
| **This work** | **0.2-22 (continuous range)** | **90** | **1.2** | **0.35-0.5** |
| Christen, ISSCC07 | 0.135,1.92,10 | 130 | 1.2 | 0.33-0.9 |
| Ouzounov, ISSCC07 | 0.1,...,10 (121 modes) | 90 | 1.2 | 0.35-1 |
| Fujimoto, ISSCC06 | 3.2,4 | 180 | 1.8 | 0.70-1.64 |
| Vadipour, VLSI08 | 0.1,0.2,1.92 | 180 | 1 | 0.72-0.91 |
| Bos, ISSCC09 | 0.1,0.5,2 | 90 | 1.2 | 0.74-2.86 |

**(b) Comparison to reconfigurable ΔΣ ADCs**

**Fig. 10** Comparison to state-of-the-art power-efficient ( FOM ≤ 2 pJ/step ) *reconfigurable*: **a)** pipelined; and **b)** ΔΣ ADCs.

## VII. Conclusion

This paper presented a pipelined ADC that is reconfigurable over a continuous range of bandwidths (0.2-22 MHz) and over multiple resolutions (10,11,12 bits). Fabricated in a 1.2-V 90-nm digital CMOS process, this ADC achieves low power (0.35 to 0.5 pJ/step) over its full bandwidth-resolution range. Accordingly, compared to state-of-the-art power-efficient *reconfigurable* pipelined or ΔΣ ADCs, this ADC provides a wide bandwidth-resolution reconfigurability space, while achieving the most competitive FOM over this full space. Furthermore, when configured to its maximum speed and maximum resolution, its FOM remains among the most competitive compared to the FOM of *non-reconfigurable* pipelined ADCs with 10.5 to 11.5 ENOBs.

## References

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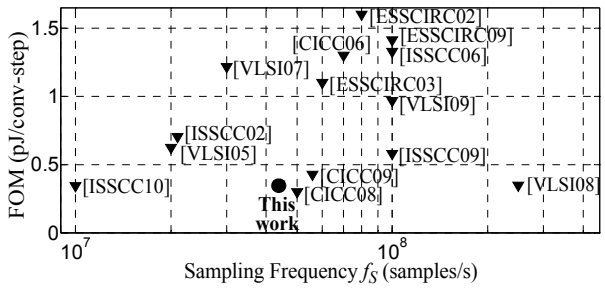


**Fig. 11** Comparison of this ADC (when reconfigured to its maximum speed and resolution) to state-of-the-art *non-reconfigurable* power-efficient ( FOM ≤ 2 pJ/step ) pipelined ADCs with *ENOB* = 10.5 to 11.5 bits (comparison limited to: ISSCC, VLSI, CICC, and ESSCIRC).