Testing Field Programmable Gate Array (FPGA) Interconnects

By Stuart McCracken

Overview

- FPGA Description and Structures
- Interconnect Structures and Types
- Testing the Interconnects

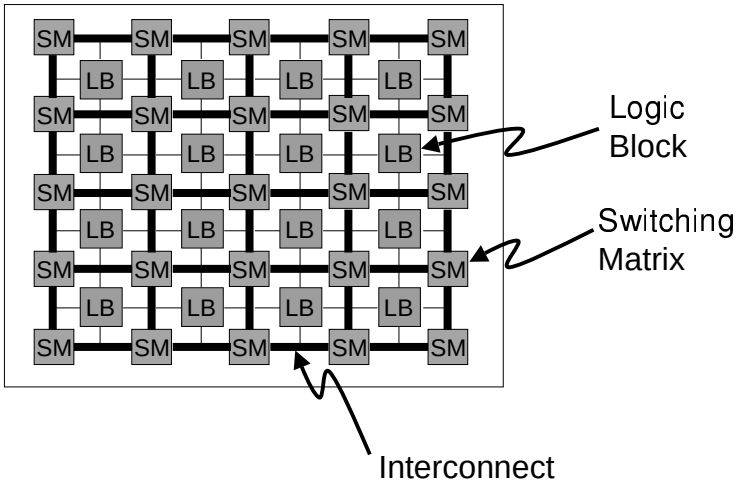
A Brief Overview of FPGA Technology

Testing FPGA Interconnects

- Extremely versatile chips allowing for a wide variety of digital designs
- Composed of 'Programmable Logic Elements' which form Logic Blocks
- Many types of structures and orderings of these logic blocks (Different companies have their own approach)
- More Info: http://www.vcc.com/fpga.html

A Brief Overview of FPGA Technology

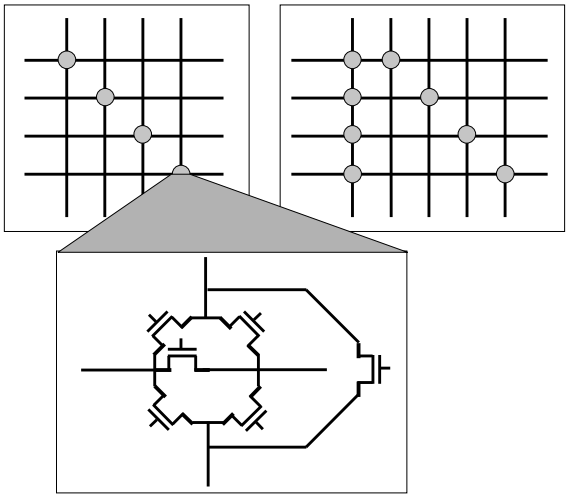
Testing FPGA Interconnects



FPGA Interconnect Structures

Testing FPGA Interconnects

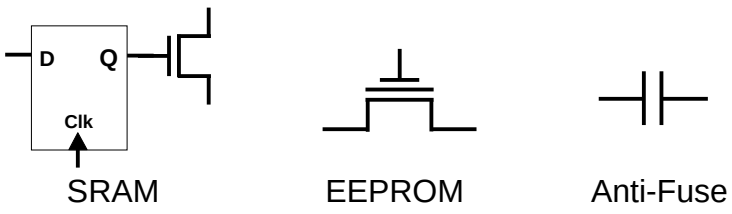
- Two examples of switching matrices



FPGA Interconnect Structures

Testing FPGA Interconnects

- Interconnections are made through pass transistors
- Pass transistors are of three main types: SRAM, EEPROM, Anti-fuse



Testing of FPGAs

- Three major aspects of FPGAs need to be tested: I/O, Logic, and Interconnect
- Programmability adds complexity to testing problem
- Re-programmability allows for an easier time in testing
- Re-programmability allows for adaptation in case of faulty FPGA

Testing of Interconnects

- Fulfilling interconnect testing can summarized as making sure a signal has been passed and tested through all pass transistors and continuous wires
- Anti-fuse interconnect type is only testable once programmed (like testing any ASIC)
- SRAM and EEPROM types can be tested through 'testing programs' to be downloaded

Testing of Interconnects

- Two main approaches have been devised:
  - Scan Based Testing via I/Os
  - Built-In Self Test (BIST)

- These testing approaches combined with the FPGA characteristics help in the pursuit of fault tolerant systems

Scan Based Testing via I/Os

- Goal is to set-up internal interconnects such that inputs are forced through I/Os and output is observed through I/Os

- Requires many different programming steps to achieve full coverage of all wires and pass transistors

- External equipment required to drive and observe stimulus and outputs

Built-In Self Testing (BIST)

- Goal is to set up a system which tests itself on-chip by producing its own test vectors and detecting errors throughout the process

- Also requires many programming steps to test all portions of the FPGA

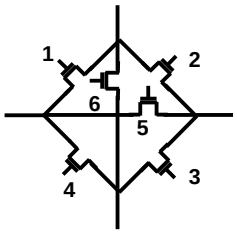
- Need to switch the testers/analyzers with units under test

- If the testers/analyzers are faulty can their tests be conclusive?

FPGA Interconnect Test Passes

- Full Testing of a Cross-Point Requires the Following Passes:

Pass 1: 1-3-6	Pass 4: 2-4-5
Pass 2: 2-4-6	Pass 5: 1-3
Pass 3: 1-3-5	Pass 6: 2-4
Pass 7: 5-6	



- Each cross-point has to be tested for defective pass transistors.
- All tests using several configurations can pin point the faulty transistor, whereas less configurations can pin point the faulty switching matrix.
- BIST or a Scan Technique can be used to test the interconnects.

Fault Tolerant FPGA Interconnect Structure

Testing FPGA Interconnects

- Adding 4 pass transistors can increase the fault tolerance of the original design.
- If T1 is faulty, T7 and T8 can be used to replace it. T5 can be replaced by T7 and T9, and so on...
- Increase in number of transistors is 66%.
- Reliability changes as in the graph.

SM = Switching Matrix
FTSM = Fault Tolerant Switching Matrix