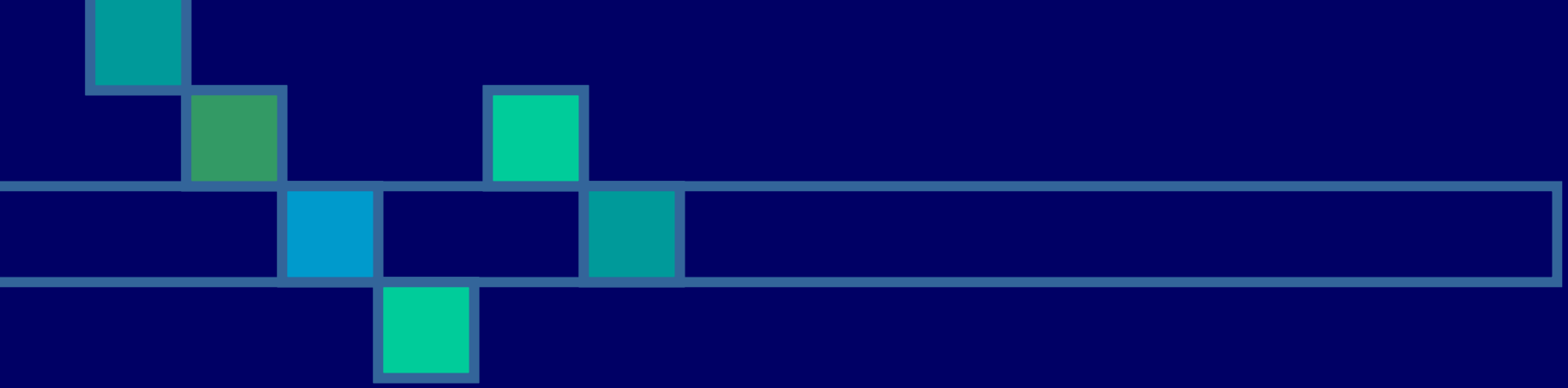


Delay Default Testing Based on Formal Verification ---- Overview

Xiaohua Kong & Lige Wang

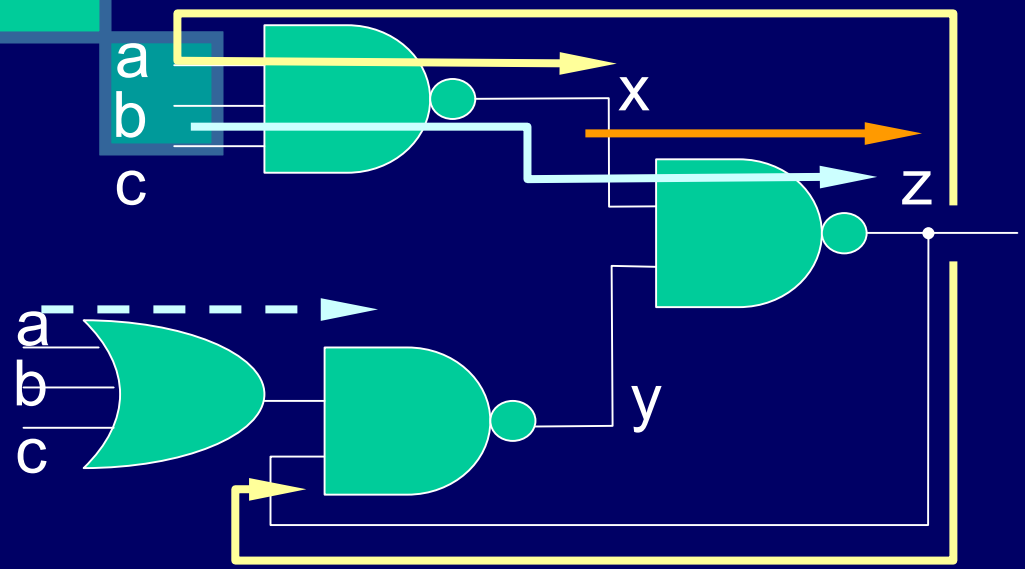
Delay Fault

- Correctness of the circuit:
  - Functional correctness.

    A circuit is said to be functionally correct if an appropriate combination of the delays of its components can produce the behavior expected by the environment.
  - **Behavioral correctness.**

    A functionally correct circuit is said to be behaviorally correct if it produces the behavior expected by the environment regardless the delay assigned for the delay models and the technology.

Behavioral Correctness VS. Functional Correctness

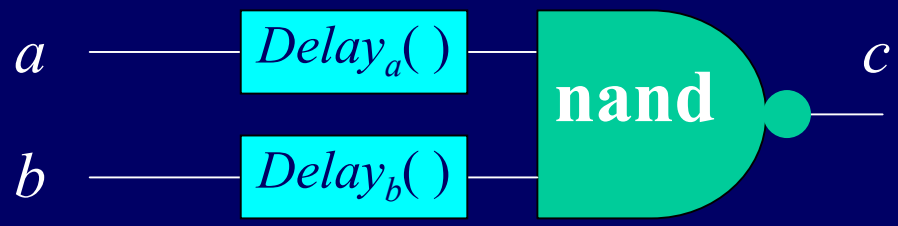


$z = abc + z\,(a+b+c)$

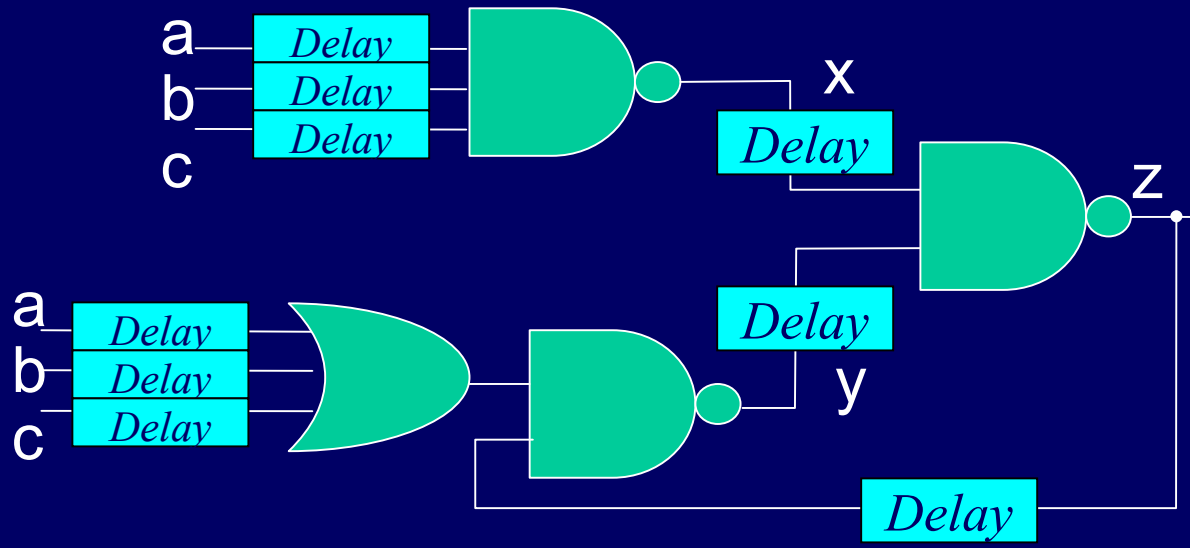
- Three input c-element.
- The logic function is correct.
- Delay fault: $D_{z+y-} > D_{z+x+}$.
- The behavior is incorrect when:

  $c+b+a+x-z+a-x+z-$.

Delay Modeling Using Processes:



One process each gate and abstract delay model.



Connection of process to construct the process of implementation.

Delay Models

- Transition fault model for individual gate
  - A logical model for a defect that delays a rising/falling transision at inputs or outputs of logic gates
  - Propagation pattern identical to DC stuck-at fault.
- Path delay fault model for implementation.
  - Any path with a total delay exceeding the system clock interval has a path delay fault

Delay models(cont'd)

- Functional sensitizable: depends on all paths
- Robust: any path combination, independent on delays

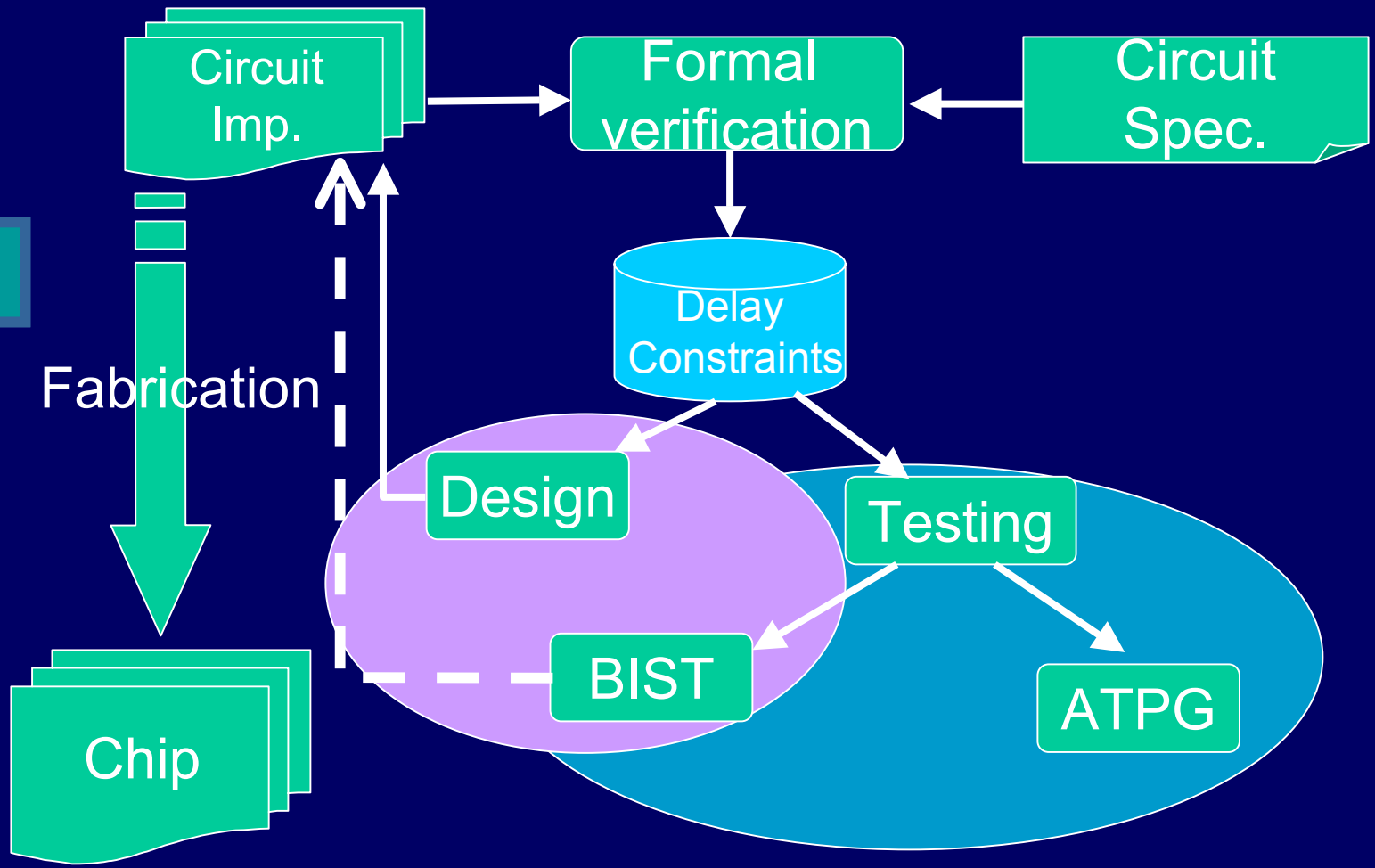
- Line Delay Model
  - Test the longest sensitizable path passing through a target line producing a rising(falling)transition on it

Weakest test.

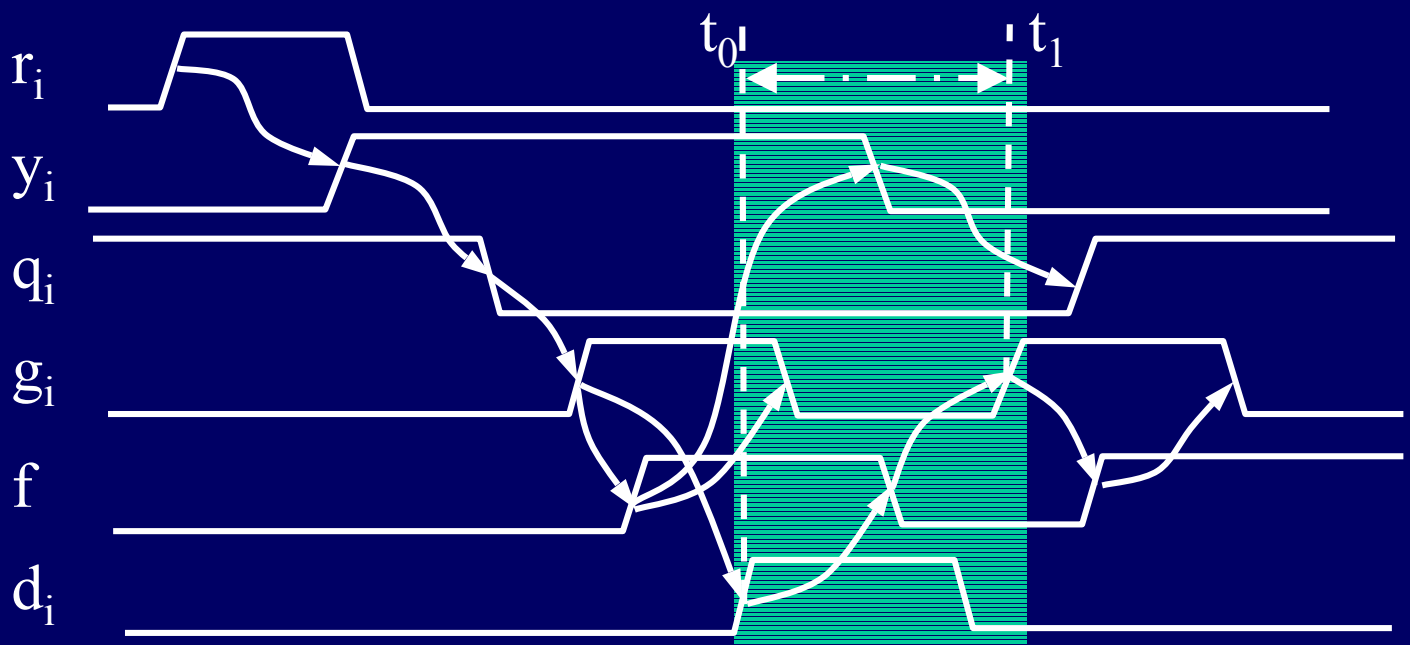
---- reuse formal verification

- Formal method to facilitate testing.
- Relative timing constraints provided by formal verification.
  - Delay model.
  - The path delay rules for correct behavior.
  - Different from critical path analysis.
- Used not only for design, but also for testing!
  - ATPG
  - BIST

Flow


Circuit Imp.
Formal verification
Circuit Spec.
Fabrication
Delay Constraints
Design
Testing
BIST
ATPG
Chip

Test Pattern Generation.
---- reuse formal verification



- Witness execution: $r_2+\ y_2+\ q_2-\ g_2+\ f+\ g_2-\ d_2+\ f-\ g_2+\ f+\ g_2-$
- Delay constraint: $D\ (g_i+\ f+\ d_i+\ f-) > D\ (g_i+\ y_i-\ q_i+)$
- Test: $(r_i+\ ,\ 0)\ (d_i+\ ,\ t_0)$; fault output is $(g_i=1\ ,\ t_1)$.

On-line BIST

---- reuse formal verification