COEN 6521
VLSI Testing
Scan Design
Zeljko Zilic
McGill University
546 McConnell Eng. Building
zeljko@ece.mcgill.ca
Remark

- Some of the material used in these slides based on slides by V. Agrawal
- sayee_su@ece.concordia.ca
Overview

- Definition
- Ad-hoc methods
- Scan design
  - Design rules
  - Scan register
  - Scan flip-flops
  - Scan test sequences
  - Overheads
  - Scan design system
- Partial Scan
Definitions

- *Design for testability* (DFT) refers to those design techniques that make test generation and test application cost-effective.

- DFT methods for digital circuits:
  - Ad-hoc methods
  - Structured methods:
    - *Scan*
    - *Partial Scan*
    - *Built-in self-test* (BIST)
    - *Boundary scan*
Ad-Hoc DFT Methods

- Good design practices learnt through experience:
  - Avoid asynchronous (unclocked) feedback.
  - Make flip-flops initializable.
  - Avoid redundant gates. Avoid large fanin gates.
  - Provide test control for difficult-to-control signals.
  - Avoid gated clocks.
  - Consider ATE requirements (tristates, etc.)

- Design reviews conducted by experts or design auditing tools

- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available
  - Test generation often manual with no guarantee of high fault coverage
  - Design iterations may be necessary
Scan Design

• Circuit designed using pre-specified design rules
• Test structure (hardware) added to the verified design:
  ✦ Adding test control (TC) primary input
  ✦ Replacing flip-flops by scan flip-flops (SFF) and connecting to form one or more shift registers in test mode
  ✦ Making input/output of each scan shift register controllable/observable from PI/PO
• Use of combinational ATPG to obtain tests for all testable faults in combinational logic
• Adding shift register tests and converting ATPG tests into scan sequences for use in manufacturing test
Scan Design Rules

- Use only clocked D-type of flip-flops for all state variables
- At least one PI pin available for test; more pins, if available, can be used
- All clocks controlled from PIs
- Clocks must not feed data inputs of flip-flops
Correcting Design Rule Violation

- All clocks controlled from PI
Scan Flip-Flops

D flip-flop

Master latch  Slave latch

D flip-flop

CK

Master open  Slave open

CK

TC

Normal mode, D selected  Scan mode, SD selected

TC
Scan Design

**PI** → **Combinational logic** → **PO**

- **SFF**
- **SCANOUT**

**SCANIN**

Not shown: CK or MCK/SCK feed all SFFs.
Testing Using Scan

Combinational logic

PI: I1 I2
SCANTIN: X
TC: X
Present state: S1 S2

Logic

Next state: N1 N2
PO: O1 O2
SCANOUT

O1 O2
Combinational Test Vectors

Sequence length = \((n_{\text{comb}} + 1) n_{\text{sff}} + n_{\text{comb}}\) clock periods

\(n_{\text{comb}} = \) number of combinational vectors
\(n_{\text{sff}} = \) number of scan flip-flops

Don’t care or random bits

[Diagram showing PI, I1, I2, SCANIN, S1, S2, TC, O1, O2, PO, N1, N2, SCANOUT]
Testing Scan Registers

- Need to test scan register prior to application of scan test sequences
- Shift sequence 00110011 . . . of length $n_{sff}+4$ in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output
- Total scan test length: $n_{sff} \times n_{comb} + 4$ clock periods
  - Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length $\sim 10^6$ clocks
- Multiple scan registers reduce test length
Multiple Scan Registers

- Possibility of distributing scan flip-flops among any number of shift registers, each having a separate scanin and scanout pin
- Test sequence length determined by the longest scan shift register
- Just one test control (TC) pin essential
Partial Scan

- Subset of flip-flops is scanned.
- Objectives:
  - Minimizing area overhead and scan sequence length, while achieving required fault coverage
  - Excluding selected flip-flops from scan:
    - Improvement of performance
    - Allowing on limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences
Partial Scan Architecture

Combinational circuit

CK1

CK2

TC

scanin

scanout

pi

po
Test Generation

- Scan and non-scan flip-flops controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active

- Seq. ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100…., of length \( n_{sff} + 4 \) applied in scan mode
  - Each ATPG vector preceded by scan-in sequence to set scan flip-flop states
  - Scan-out sequence added at the end of each vector sequence

- Test length = \((n_{ATPG} + 2) \ n_{sff} + n_{ATPG} + 4\) clocks
Flip-Flop for Partial Scan

- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop used
- Scan flip-flops required separate clock control:
  - Either separate clock pin
  - Or alternative design for a single clock pin
Why Partial Scan

- Generalized scan method; scan varying from 0 to 100%
- Partial-scan has lower overheads (area and delay) and reduced test length
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned
Motivation for Boundary Scan Standard

- Components put on both sides of PCB
- Reduced spacing between PCB wires
- PCB tester replaced with build-in test delivery system - JTAG
  - Need to add standard System Test Port and Bus to provide I/O communication
- Components on PCB from different vendors
  - Test bus identical for various components
  - One chip providing test hardware for other chips
Purpose of Standard

- Test instructions and data serially fed into CUT
  - Possibility to read out test results
  - Too many shifts to shift in external tests
- JTAG controlling scan operation on chip, PCB and system level
- Characteristics
  - Control of tri-state signals during testing
  - Other chips used to collect test responses from CUT
  - System interconnects to be tested separately from components
  - Components tested separately from wires
System Test Logic

- Boundary Register Cell
  - Boundary Register

- System Circuitry
  - Device ID Register
  - Bypass Register
  - Instruction Register (Control Signals)
  - TAP Controller

- System I/O
  - TDI
  - TCK
  - TMS
  - TRST*
Interconnects at System Level
Boundary Scan Chain

Input Pin

On-Chip System Logic

From TDI

Pl
Si
PO

To TDO

Pl
Si
PO

Pl
Si
PO

Pl
Si
PO

Pl
Si
PO

Pl
Si
PO

Pl
Si
PO

3-State Pin

2-State Pin

Bidirectional Pin

On-Chip System Logic
Boundary Scan Cell
Serial Board Scan

Diagram showing the connections between chips and test circuitry, including TDI (Serial data in), TDO (Serial data out), TCK (Test clock), and TMS (Test mode select) signals. The diagram illustrates the serial test interconnect and system interconnect.
Parallel Board Scan
Independent Path Board Scan
Signals at Test Access Port (TAP)

- **Test Clock Input (TCK)** - Clock for test logic
  - Possibly running at different rate than system clock

- **Test Mode Select (TMS)** - Switching system from functional to test mode

- **Test Data Input (TDI)** - Accepting serial test data and instructions
  - Used to shift-in vectors or one of many test instructions

- **Test Data Output (TDO)** - Serially shifting-out test results captured in boundary scan chain (or device ID or other internal register)

- **Test Reset (TRST)** - Optional asynchronous TAP controller reset
State Diagram of TAP Controller